Patent
Attorney's Docket No. MP0071

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	Examiner: Justin King
Yat-Tung LAM, et al.	)	Group Art Unit: 2111
Application No.: 09/759,151	)	Appeal No. _____
Filed: January 16, 2001	)	Confirmation No.: 4662
For: LONG LATENCY INTERFACE PROTOCOL	)	Date: July 20, 2005

BRIEF FOR APPELLANT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal is from the decision of the Patent Examiner dated April 20, 2005, finally rejecting Claims 1-11, 15-25, 31-41, 46-56, 60-71, 76-86, 91-104, 106, 107, 121-131, 135, 136, 151-161, and 212-222, which are reproduced as an Appendix to this Appeal Brief.

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I. Real Party in Interest

The entire interest in the present application, and the invention to which it is directed, is assigned to Marvell International Ltd., as recorded in the Patent and Trademark Office at Reel 011479, Frame 0777 and Reel 011479, Frame 0768.

II. Related Appeals and Interferences

The Appellants' legal representative and assignee do not know of any other appeals or interferences which will directly affect, or be directly affected by, or have a bearing on the Board's decision in this Appeal.

III. Status of Claims

The present application contains claims 1-11, 15-25, 31-41, 46-56, 60-71, 76-86, 91-104, 106, 107, 121-131, 135, 136, 151-161, and 212-222, all of which are currently pending. Claims 12-14, 26-30, 42-45, 57-59, 72-75, 87-90, 105, 108-120, 132, 134, 137-150, 162-211, and 223-247 have been canceled. Claims 1-11, 15-25, 31-41, 46-56, 60-71, 76-86, 91-104, 106, 107, 121-131, 135, 136, 151-161, and 212-222 form the basis for this Appeal.

IV. Status of Amendments

No amendments or responses were filed subsequent to final rejection.

V. Summary of the Invention

The present invention relates to a versatile, latency-independent interface between hardware components, such as between a read/write (R/W) channel or read channel (RDC) and a hard disk controller (HDC). [*see* present application, page 1, paragraph 0005]

Referring to Figure 1 of the present application, a typical disk drive system includes a hard disk controller (HDC) 12 that interfaces with a R/W channel or RDC 14 which is in communication with a disk 16. Data transfer between HDC 12 and the R/W channel 14 is synchronized by read gate (RGATE) and write gate (WGATE) control signals. In a read operation, R/W channel 14 processes an incoming analog signal from a disk 16, and transfers the data to he HDC 12. In a write operation, data is transferred from HDC 22 to the R/W channel to be written to the disk. Latency refers to the time or byte delay that data remains in the R/W channel. Some disk drive systems have latencies of about 20 bytes which, depending on the particular system, amounts to a time delay of between about 800 ns and 5 ms. [*see* present application, page 1, paragraph 0007 to page 2, paragraph 0008]

Technology such as iterative turbo coding, which is being introduced into modern disk drive systems, requires more processing before the data is available, which, in turn, requires R/W channels or RDCs with higher latencies. One problem is that the interface used in the shorter latency systems is not capable of supporting the higher latencies. Accordingly, a new interface is needed that supports higher latency R/W channel or RDC designs. [*see* present application, page 1, paragraph 0007 to page 2, paragraph 0008]

The prior art disk drive systems simply cannot handle the higher latency requirements of, for example, iterative turbo decoding. The system and methods of the present invention, however, can accommodate higher latency read/write or read channels by using, for example, the serial data control signal that includes information such as non-split, first-split, continue-split and last-split that pertains to the data being read from or written to the disk. The system according to exemplary embodiments further provides a flexible interface to support the

higher read and write latencies of greater than one sector, a split sector format, and a second sector mark.

To address the above described problems, according to a first exemplary embodiment of the present invention, as recited in, for example, independent claims 1, 31, 46, 76, 121, and 151, a latency-independent interface between first and second hardware components 22, 24 is provided. The latency-independent interface includes a serial control data circuit 70, 42 that transmits and receives a serial control data signal (SCD) and a data circuit 78, 50 that transmits or receives data (e.g., NRZ[8:0]) under the control of the serial data gate signal (e.g., RWGate) [*see* present application, pages 6 and 7, paragraph 0066, Figure 2, pages 7, 8, paragraph 0070, and page 10, paragraph 0077]. The serial control data signal includes information as to whether the data is one of split and non-split. [*see* present application, Figure 2, page 7, paragraph 0070, pages 8 and 9, Table 1, pages 10 and 11, and paragraph 0079] Furthermore, the first and second hardware components, 22, 24 can include a hard disk controller and a read channel. [*see* present application, Figure 1, page 6, paragraph 0058]

According to a second aspect of the present invention, as recited in, for example, independent claims 2, 32, 47, 77, 92, 107, 122, 152, and 213, a latency-independent interface between first and second hardware components 22, 24 includes a serial control data circuit 70, 42 that transmits and receives a serial control data signal (SCD) and a data circuit 78, 50 that transmits or receives data (e.g., NRZ[8:0]) under the control of the serial data gate signal (e.g., RWGate). [*see* present application, page 6, 7, paragraph 0066, Figure 2, pages 7, 8, paragraph 0070, and page 10, paragraph 0077] The serial control data signal includes information as to whether the data is one of split and non-split. [*see* present application, Figure 2, page 7, paragraph 0070, Table 1, and pages 10 and 11, paragraph 0079] The serial control data signal includes the serial control data signal (SCD) that includes information that the data is one of a first split, continue split and last split. [*see* present application, pages 8 and 9, Table 1, Figure 5, page 11, paragraph 0083, Figure 9, pages 12 and 13, paragraph 88, Fig, 29, and page 28, paragraph 162]

According to a third aspect of the present invention, as recited in, for example, independent claims 6, 36, 51, 81, 96, 111, 126, and 217, a latency-independent interface between first and second hardware components 22, 24 is provided. The latency-independent

interface includes a serial control data circuit 70, 42 that transmits and receives a serial control data signal (SCD) and a data circuit 78, 50 that transmits or receives data (e.g., NRZ[8:0]) under the control of the serial data gate signal (e.g., RWGate). [*see* present application, page 6, 7, paragraph 0066, Figure 2, pages 7, 8, paragraph 0070, and page 10, paragraph 0077] The serial control data signal includes information as to whether the data is one of split and non-split. [*see* present application, Figure 2, page 7, paragraph 0070, Table 1, and pages 10 and 11, paragraph 0079] Furthermore, the serial data signal includes information if a succeeding serial control data signal is a continuation of a preceding serial control data signal. [*see* present application, pages 7, paragraph 70, page 11, paragraph 80, and Figure 3]

According to a further aspect of the present invention, a latency-independent interface between first and second hardware components 22, 24 includes a serial control data circuit 70, 42 that transmits a serial control data signal (SCD), a data circuit 78, 50 that transmits or receives data (e.g., NRZ[8:0]) under the control of the serial control data signal, and a sync mark transceiver 76, 48 that transmits or receives sync mark information (e.g., SM_DET, or SM_ST). [*see* present application, page 10, paragraph 0077] During a write operation, a first assertion by the first hardware component 22 of the sync mark information indicates a start of sync mark insertion, and a second assertion by the first hardware component of the sync mark information indicates a start of writing of padding data. [*see* present application, page 9, paragraph 0074] During a read operation, an assertion by the second hardware component 24 information indicates that a sync mark was detected. [*see* present application, page 9, paragraph 0075]

According to a fourth aspect of the present invention, as recited in, for example, independent claims 8, 22, 38, 53, 67, 83, 98, 113, 128, 142, 158, and 219, a latency-independent interface between first and second hardware components 22, 24 includes a serial control data circuit 70, 42 that transmits a serial control data signal (SCD), a data circuit 78, 50 that transmits or receives data (e.g., NRZ[8:0]) under the control of the serial data gate signal (e.g., RWGate), and a ready transceiver 66,38 that transmits or receives a ready signal (e.g., RC_RDY, or HDC_RDY). [*see* present application, pages 6 and 7, paragraph 0066, and page 7, paragraph 0069] The serial control data signal includes information as to whether the

data is one of split and non-split. [*see* present application, page 2, Figure 2, page 7, paragraph 0070, pages 10 and 11, paragraph 0070, and Table 1] During a write operation, the ready signal (e.g., RC_RDY) indicates the second hardware component 24 is ready to receive data from the first hardware component 22, and during a read operation, the ready signal (e.g., HDC_RDY) indicates the first hardware component 22 is ready to receive data from the second hardware component 24. [*see* present application, pages 6 and 7, paragraph 0066, and page 7, paragraph 0069]

According to another aspect of the present invention, as recited in, for example, independent claims 5, 19, 35, 50, 64, 80, 95, 110, 125, 139, 155, and 216, a latency-independent interface between first and second hardware components 22, 24 includes a serial control data circuit 70, 42 that transmits and receives a serial control data signal (SCD) and a data circuit 78, 50 that transmits or receives data (e.g., NRZ[8:0]) under the control of the serial data gate signal (e.g., RWGate) [*see* present application, pages 6 and 7, paragraph 0066, Figure 2, pages 7, 8, paragraph 0070, and page 10, paragraph 0077]. The serial control data signal includes information as to whether the data is one of split and non-split. [*see* present application, Figure 2, page 7, paragraph 0070, Table 1, pages 10 and 11, and paragraph 0079] The serial control data signal also includes a codeword size of a current sector. [*see* present application, pages 8 and 9, Table 1, page 11, paragraph 0081, and pages 11, paragraph 0083] Additionally, the serial control data signal can include an amount of data to be written during a write operation, and an amount of data to be read during a read operation. [*see* present application, pages 8 and 9, Table 1]

According to a still further aspect of the present invention, a computer program for transmitting and receiving signals between first and second hardware components 22, 24 includes the steps of receiving a serial control data signal (SCD) and transmitting or receiving data (NRZ[8:0]) under the control of the serial control data signal. The serial control data signal includes information as to whether the data is one of split and non-split. [*see* present application, page 2, paragraph 0010, Figure 2, page 7, paragraph 0070, Table 1, and page 41, paragraph 231]

Independent claims 15, 16, 19, 20, and 22 of the present application recite the feature of "serial control transmitting means for transmitting a serial control data signal." For

purposes of illustration, the structure described in the specification as corresponding to the claimed function can be shown as, for example, an SCD transceiver, such as, for example, SCD transceiver 70, 42 illustrated in Figure 2, and described at page 6, paragraph 58, pages 7 and 8, paragraph 70, and pages 10 and 11, paragraphs 77-80.

Independent claims 60, 61, 64, 65, and 67 of the present application recite the feature of "serial control receiving means for receiving a serial control data signal." For purposes of illustration, the structure described in the specification as corresponding to the claimed function can be shown as, for example, an SCD transceiver, such as, for example, an SCD transceiver 70, 42 illustrated in Figure 2, and described at page 6, paragraph 58, pages 7 and 8, paragraph 70, and pages 10 and 11, paragraphs 77-80.

Independent claims 15, 16, 19, 20, 22, 60, 61, 64, 65, and 67 of the present application recite the feature of "data transceiver means for transmitting or receiving data under the control of the serial control data signal." For purposes of illustration, the structure described in the specification as corresponding to the claimed function can be shown as, for example, a data transceiver, such as, for example, a data transceiver 78, 50 illustrated in Figure 2, and described at page 6, paragraph 58, pages 7 and 8, paragraph 70, and pages 10 and 11, paragraphs 77-80.

Independent claims 22 and 67 of the present application further recite the feature of "a ready transceiver means for transmitting or receiving a bi-directional ready signal." For purposes of illustration, the structure described in the specification as corresponding to the claimed function can be shown as, for example, a ready transceiver, such as, for example, a ready transceiver 66, 38 illustrated in Figure 2, and described at page 6, paragraph 58, pages 7, paragraph 69, and page 10, paragraphs 77 and 78.

Dependent claim 24 and 69 recites the feature of a "sync mark transceiver means for transmitting or receiving sync mark information." For purposes of illustration, the structure described in the specification as corresponding to the claimed function of the sync mark transceiver means can be shown as, for example, a sync mark transceiver, such as, for example, a sync mark transceiver 76, 48 illustrated in Figure 2, and described at page 9, paragraphs 74 and 75, and page 10, paragraphs 77 and 78.

Independent claims 135, 136, 139, 140, and 142 of the present application recite the features of a "first component means comprising serial control transmitter means for transmitting a serial control data signal and first data transceiver means for transmitting or receiving data under the control of the serial control data signal." For purposes of illustration, the structure described in the specification as corresponding to the claimed function of the serial control transmitter means can be shown as, for example, an SCD transceiver, such as, for example, an SCD transceiver 70 illustrated in Figure 2, and described at page 6, paragraph 58, pages 7 and 8, paragraph 70, and pages 10 and 11, paragraphs 77-80. For purposes of illustration, the structure described in the specification as corresponding to the claimed function of the first data transceiver means can be shown as, for example, a data transceiver, such as, for example, a data transceiver 78 illustrated in Figure 2, and described at page 6, paragraph 58, pages 7 and 8, paragraph 70, and pages 10 and 11, paragraphs 77-80.

Independent claims 135, 136, 139, 140, and 142 of the present application further recite the features of a "second component means comprising serial control receiver means for transmitting a serial control data signal and second data transceiver means for transmitting or receiving data under the control of the serial control data signal." For purposes of illustration, the structure described in the specification as corresponding to the claimed function of the serial control receiver means can be shown as, for example, an SCD transceiver, such as, for example, an SCD transceiver 42 illustrated in Figure 2, and described at page 6, paragraph 58, pages 7 and 8, paragraph 70, and pages 10 and 11, paragraphs 77-80. For purposes of illustration, the structure described in the specification as corresponding to the claimed function of the second data transceiver means can be shown as, for example, a data transceiver, such as, for example, a data transceiver 50 illustrated in Figure 2, and described at page 6, paragraph 58, pages 7 and 8, paragraph 70, and pages 10 and 11, paragraphs 77-80.

Independent claim 142 of the present application further recites the feature of a "first ready transceiver means for transmitting or receiving a bi-directional ready signal," and the feature of a "second ready transceiver means for transmitting or receiving the bi-directional ready signal." For purposes of illustration, the structure described in the specification as corresponding to the claimed function of the first and second ready transceiver means can be

shown as, for example, a ready transceiver, such as, for example, a first and second ready transceivers 66, 38, respectively, illustrated in Figure 2, and described at page 6, paragraph 58, pages 7, paragraph 69, and pages 10, paragraphs 77 and 78.

Dependent claim 144 recites the features of a "first sync mark transceiver means for transmitting and receiving sync mark information," and a "second sync mark transceiver means for transmitting and receiving the sync mark information." For purposes of illustration, the structure described in the specification as corresponding to the claimed function can be shown as, for example, a sync mark transceiver, such as, for example, a first and second sync mark transceivers 76, 48, respectively, illustrated in Figure 2, and described at page 9, paragraphs 74 and 75, and page 10, paragraphs 77 and 78.

VI. Grounds of Rejection to be Reviewed on Appeal

The final Office Action presents eight grounds of rejection for review in this Appeal:

1. Claims 1, 15, 31, 46, 60, 76, 91, 106, 121, 135, 151, and 212 stand finally rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over the combination of the Admitted Prior Art in view of Sharma et al. (U.S. Patent No. 6,636,906, hereinafter "Sharma").

2. Claims 2, 16, 32, 47, 61, 77, 92, 107, 122, 136, 152, and 213 stand finally rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over the combination of the Admitted Prior Art in view of Sharma.

3. Claims 6, 20, 36, 51, 65, 81, 96, 111, 126, 140, 156, and 217 stand finally rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over the combination of the Admitted Prior Art in view of Sharma.

4. Claims 9, 23, 39, 54, 68, 84, 99, 114, 129, 143, 159, 220, 252, 258, 264, 270, 276, 282, 288, 294, 300, 306, 312, 318, 324, 330, 336, 342, 348, 354, 360, and 366 stand finally rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over the combination of the Admitted Prior Art in view of Sharma.

5. Claims 3, 4, 17, 18, 33, 34, 48, 49, 62, 63, 78, 79, 93, 94, 108, 109, 123, 124, 137, 138, 153, 154, 214, 215, 249, 250, 255, 256, 261, 262, 267, 268, 276, 274, 279, 280, 285, 286, 291, 292, 297, 298, 303, 304, 309, 310, 315, 316, 321, 322, 327, 328, 333, 334, 339, 340, 345, 346, 351, 352, 357, 358, 363, 364, 369, 371, 373, and 375 stand finally rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over the combination of the Admitted Prior Art in view of Dunn et al. (U.S. Patent No. 5,274,772 hereinafter "Dunn").

6. Claims 5, 19, 35, 50, 64, 80, 95, 110, 125, 139, 155, and 216 stand finally rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over the combination of the Admitted Prior Art in view of Dunn.

7. Claims 8, 22, 38, 53, 67, 83, 98, 113, 128, 142, 158, and 219 stand finally rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over the combination of the Admitted Prior Art in view of Dunn.

8. Claims 7, 21, 37, 52, 66, 82, 97, 112, 127, 141, 157, 218, 10, 24, 40, 55, 69, 85,100, 115, 130, 144, 160, 221 11, 25, 41, 56, 70, 86, 101, 116, 131, 145, 161, 222, 215, 253, 254, 257, 259, 260, 263, 265, 266, 271, 272, 275, 277, 278, 281, 283, 284, 287, 289, 290, 293, 295, 296, 299, 301, 302, 305, 307, 308, 311, 313, 314, 317, 319, 320, 323, 325, 326, 329, 331, 332, 336, 337, 338, 341, 343, 344, 347, 349, 350, 353, 355, 356 ,359 ,361, 362, 365, 367, 368, 370, 372, 374, and 376 stand finally rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over the combination of the Admitted Prior Art in view of Dunn further in view of Bliss et al. (U.S. Patent No. 6,009,549 hereinafter "Bliss").

VII. Arguments

A. Summary of Arguments

For the convenience of the Board, a summary of Appellants' arguments in response to the aforementioned grounds of rejection is provided below. The following arguments are discussed in greater detail in Sections VII.B - VII.I.

1. Rejection of Claims 1, 15, 31, 46, 60, 76, 91, 106, 121, 135, 151, and 212 Under 35 U.S.C. § 103(a) as Allegedly Being Unpatentable Over the Combination of the Admitted Prior Art In View of Sharma.

These claims recite the feature of, for example, a serial control data signal comprising information as to whether the data is one of a split or non-split, as recited in at least independent claim 1, among others. The combination of the Admitted Prior Art and Sharma, alone or in combination, does not disclose or suggest at least the claim feature of the serial control data signal comprising information as to whether the data is one of a split or non-split. The Patent Office attempts to show that a combination of features disclosed by the Admitted Prior Art and Sharma is "equivalent" to the Appellants' claimed feature, but is unsuccessful in that there is neither a legal basis for such combination, nor factual, as important elements of the claimed feature are missing from the combination.

There is no motivation or suggestion, found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the prior art or to combine the prior art. The Patent Office admits that "any judgment on obviousness is in a sense necessarily a reconstruction based upon *hindsight reasoning*." [Final Office Action, page 7, emphasis added] Hindsight reasoning by the Patent Office is impermissible. [*see* M.P.E.P. § 2142]

2. Rejection of Claims 2, 16, 32, 47, 61, 77, 92, 107, 122, 136, 152, and 213 Under 35 U.S.C. § 103(a) as Allegedly Being Unpatentable Over the Combination of the Admitted Prior Art In View of Sharma.

These claims recite the feature of, for example, a serial control data signal that comprises information that the data is one of a first split, continue split, and last split. Neither the Admitted Prior Art nor Sharma discloses or suggests at least the claim feature of a serial control data signal that comprises information that the data is one of first split, continue split, and last split. Without support of any kind, the Patent Office proffers that the split read transaction disclosed by Sharma, along with a transaction identifier, somehow inherently discloses a continue split. The Patent Office has provided absolutely no stated motivation for combining Sharma with the Admitted Prior Art.

3. Rejection of Claims 6, 20, 36, 51, 65, 81, 96, 111, 126, 140, 156, and 217 Under 35 U.S.C. §103(a) as Allegedly Being Unpatentable Over the Combination of the Admitted Prior Art In View of Sharma.

These claims recite the feature of, for example, a serial control data signal that comprises information if a succeeding serial control data is a continuation of a current serial control data. Neither the Admitted Prior Art nor Sharma discloses or suggests at least the claim feature of a serial control data signal that comprises information if a succeeding serial control data is a continuation of a current serial control data. Further, the Patent Office has made no showing, whatsoever, of a motivation to combine based on actual, specific evidence.

4. Rejection of Claims 9, 23, 39, 54, 68, 84, 99, 114, 129, 143, 159, 220, 252, 258, 264, 270, 276, 282, 288, 294, 300, 306, 312, 318, 324, 330, 336, 342, 348, 354, 360, and 366 Under 35 U.S.C. §103(a) as Allegedly Being Unpatentable Over the Combination of the Admitted Prior Art In View of Sharma.

The Patent Office has failed to make any showing of a motivation to combine based on actual, specific evidence to combine the Admitted Prior Art and Sharma.

5. Rejection of Claims 3, 4, 17, 18, 33, 34, 48, 49, 62, 63, 78, 79, 93, 94, 108, 109, 123, 124, 137, 138, 153, 154, 214, 215, 249, 250, 255, 256, 261, 262, 267, 268, 276, 274, 279, 280, 285, 286, 291, 292, 297, 298, 303, 304, 309, 310, 315, 316, 321, 322, 327, 328, 333, 334, 339, 340, 345, 346, 351, 352, 357, 358, 363, 364, 369, 371, 373, and 375 Under 35 U.S.C. § 103(a) as Allegedly Being Unpatentable Over the Combination of the Admitted Prior Art In View of Dunn.

These claims recite the feature of, for example, a serial control data signal that comprises an amount of data to be written during a write operation, or an amount of data to be read during a read operation. The Patent Office admits that "[t]he [admitted] prior art does not explicitly disclose specifying the amount of the data or codeword in each session is a common practice in constructing data packets." The Patent Office has made no attempt to show where in either the Admitted Prior Art or Dunn is disclosed the claim feature of a serial control data signal comprising an amount of data to be written during a write operation, or an amount of data to be read during a read operation. The Patent Office has made no showing, whatsoever, of a motivation to combine based on actual, specific evidence.

6. Rejection of Claims 5, 19, 35, 50, 64, 80, 95, 110, 125, 139, 155, and 216 Under 35 U.S.C. § 103(a) as Allegedly Being Unpatentable Over the Combination of the Admitted Prior Art In View of Dunn.

These claims recite the feature of, for example, a serial control data signal that comprises an amount of data to be written during a write operation, or an amount of data to be read during a read operation. The Patent Office admits that "[t]he prior art does not explicitly disclose specifying the amount of the data or codeword in each session is a common practice in constructing data packets." Furthermore, the Appellants respectfully submit that the number of packets (PKT CNT) is not the same as the codeword size of a current sector.

The Patent Office cites no evidence in support of the motivation it provides that transmission efficiency can be improved by controlling the data amount in each sessions. The alleged motivation the Patent Office provides for combining the Admitted Prior Art and Dunn is nothing more than the alleged benefits of the Dunn invention.

7. Rejection of Claims 8, 22, 38, 53, 67, 83, 98, 113, 128, 142, 158, and 219 Under 35 U.S.C. § 103(a) as Allegedly Being Unpatentable Over the Combination of the Admitted Prior Art In View of Dunn.

These claims recite the feature of, for example, a ready transceiver that transmits or receives a bi-directional ready signal. The Patent Office admits that the Admitted Prior Art does not disclose or suggest either a ready signal, or a ready transceiver that transmits or receives a bi-directional ready signal. It is respectfully submitted that nowhere does Dunn disclose or suggest the feature of a ready transceiver that transmits or receives a bi-directional ready signal. The Patent Office has made no showing, whatsoever, of a motivation to combine based on actual, specific evidence.

8. Rejection of Claims 7, 21, 37, 52, 66, 82, 97, 112, 127, 141, 157, 218 10, 24, 40, 55, 69, 85,100, 115, 130, 144, 160, 221 11, 25, 41, 56, 70, 86, 101, 116, 131, 145, 161, 222, 215, 253, 254, 257, 259, 260, 263, 265, 266, 271, 272, 275, 277, 278, 281, 283, 284, 287, 289, 290, 293, 295, 296, 299, 301, 302, 305, 307, 308, 311, 313, 314, 317, 319, 320, 323, 325, 326, 329, 331, 332, 336, 337, 338, 341, 343, 344, 347, 349, 350, 353, 355, 356 ,359 ,361, 362, 365, 367, 368, 370, 372, 374, and 376 Under 35 U.S.C. § 103(a) as Allegedly Being Unpatentable Over the Combination of the Admitted Prior Art In View of Dunn, further in view of Bliss et al. (U.S. Patent No. 6,009,549, hereinafter "Bliss").

These claims recite the feature of, for example, a serial control data signal comprising during a write operation information as to a start of a sync mark and a start of a write padding data, and during a read operation information that a sync mark was detected. The Patent Office admits that "[t]he prior art does not explicitly disclose the padding data and sync mark." [Final Office Action, page 5]. Further, the Patent Office has completely and utterly failed to show how Dunn discloses or suggests the claimed feature of a serial control data signal comprising during a write operation information as to a start of a sync mark and a start of a write padding data, and during a read operation information that a sync mark was detected. Furthermore, the Patent Office asserts that Bliss teaches the sync transceiver and cites Figure 4, structure 4 of Bliss, which, upon inspection, merely reveals a sync detector. The Patent Office has made no showing of motivation to combine based on actual, specific evidence. The Patent Office offers, as a motivation to combine the references, the supposed benefits of the Dunn reference. Further, the Patent Office provides as a motivation to combine Bliss with the Admitted Prior Art and Dunn the supposed benefits of Bliss. The Patent Office has not provided any reasons to combine the prior art references based on actual, specific evidence.

B. Rejection of Claims 1, 15, 31, 46, 60, 76, 91, 106, 121, 135, 151, and 212 Under 35 U.S.C. § 103(a) as Allegedly Being Unpatentable Over the Combination of the Admitted Prior Art In View of Sharma.

It is respectfully submitted that the combination of the Admitted Prior Art and Sharma does not disclose or suggest a latency-independent interface between first and second hardware components, comprising a serial control data circuit that transmits a serial control data signal, and a data circuit that transmits or receives data under the control of the serial control data gate signal, wherein *the serial control data signal* comprises information as to whether the data is *one of split and non-split.*

1. The Admitted Prior Art

As is illustrated in Figure 1 of the present application, a typical disk drive system includes a hard disk controller (HDC) 12 that interfaces with a R/W channel or RDC 14 that is in communication with a disk 16. Data transfer between HDC 12 and the R/W channel is synchronized by read gate (RGATE) and write gate (WGATE) control signals. In a read operation, R/W channel 14 processes an incoming analog signal from disk 16 and transfers the data to HDC 12. In a write operation, data is transferred from HDC 12 to the R/W channel to be written to the disk. [*see* present application, paragraph 7, pages 1-2]

2. The Sharma Patent

As understood by the Appellants, Sharma is directed towards a snapshot mechanism that includes an apparatus and method for tracking DMA read requests for cacheable data that can be altered before the data is returned to a requesting I/O device. Attributes that uniquely identify the original I/O device and DMA read request are stored in a cache tag unit. A read lock is set when a request is made to obtain the requested data when it is not resident in a local cache. When the cache line containing the requested data is snooped out and the read

lock is set, then the cache line is set in a snapshot state. The snapshot state assures that only the original I/O device receives the read data when it has been altered subsequent to the time the original DMA read request was made. Once the data is returned to the original I/O device, the cache line is invalidated in order to prevent another I/O device from reading the stale data. [*see* Sharma, Abstract]

3. The Combination of the Admitted Prior Art and Sharma Does Not Disclose or Suggest All of the Claim Features of Claims 1, 15, 31, 46, 60, 76, 91, 106, 121, 135, 151, 212.

Even if one were to combine the Admitted Prior Art with Sharma, as suggested by the Patent Office, the rejection of the claims is still improper because the proposed combination of references does not disclose all of the features of the aforementioned claims. To establish a *prima facie* case of obviousness, the prior art must disclose or suggest all of the limitations of the claims. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). The Appellants respectfully submit that the Patent Office has failed to provide evidence that at least the feature of a serial control data signal that comprises information as to whether data is one of split or non-split is disclosed in or suggested by any of the cited references.

As acknowledged by the Patent Office, *nowhere* does the Admitted Prior Art disclose or suggest the feature of *a serial control data signal* that comprises information as to whether the data is *one of split and non-split*. [*see* Final Office Action, page 2]

Additionally, the Patent Office states that column 1, lines 36-37, of Sharma, "discloses a method of solving the latency problem in I/O operations caused by devices." [Final Office Action, pages 2 and 3] Contrary to the assertions of the Patent Office, column 1, lines 36-37, of Sharma merely identifies the problem with latency and the source of the problem:

> [a] problem that often arises in a cache coherent I/O system is the increased latency time that is involved in accessing the data when it does not reside in the cache associated with the requesting I/O device. This latency *may be attributed* to a remote source that has the data *and may also be* due to the bus protocol used by the requesting I/O device. [Sharma, Column 1, lines 36-37 (emphasis added)]

The Patent Office's citation to Sharma above merely reflects that Sharma has identified a problem, and may have identified the source of the problem. But in no way, shape or form, has Sharma provided even one word as to a possible solution.

The Patent Office then states that "Sharma teaches one to obtain the data value at the time the request was made and to make forward progress without incurring delay attributable to obtaining the updated value." [Office Action, page 3, citing Sharma, column 2, lines 15-21] Respectively, the Appellants submit that this is unrelated to the claimed feature of a serial control data signal that comprise information as to whether the data is one of split and non-split. Further, the Patent Office then states that "Sharma discloses that it is known to *indicate* whether the transaction is split or non-split," [Office Action page 3 (emphasis added)], and cites column 6, lines 35-37. This simply is incorrect on several accounts.

The aforementioned citation to Sharma states that "[t]he start address 164 and the byte enable 170 information *is stored* in order to uniquely identify the original request in the case of a *non-split* read transaction." [Sharma, column 6, lines 35-37 (emphasis added)] First, Sharma only discloses storing information as to *non-split-read data*. Sharma mentions nothing whatsoever about split versus non-split data. Second, Sharma provides no signal that contains information as to whether the data is one of split or non-split. Sharma merely *stores* the data about non-split read transactions.

The Patent Office then concludes that "Sharma's means to control the split transaction activities is equivalent to the claimed serial control data signal." [Final Office Action, page 3] The Patent Office bases this unfounded assertion on the grounds that "Sharma teaches one to obtain the data value at the time the request was made and to make forward progress without incurring delay attributable to obtaining the updated value . . Sharma teaches an embodiment with splitting transactions . . [and] Sharma discloses that it is known to indicate whether the transaction is split or non-split." [Final Office Action, pages 2 and 3] It is respectfully submitted, however, that the Patent Office does not and cannot point to any disclosure of Sharma that teaches that the combination of the different steps disclosed in Sharma of obtaining the data value at the time the request was made and to make forward progress with incurring a delay attributable to obtaining the updated value, accommodating

split read transactions that are supported by other bus architectures, and knowing whether a transaction is split or non-split is equivalent to the serial control data signal feature of the Appellants' claimed invention. It is as if the Patent Office is stating that the claimed feature of a serial control data signal that comprises information as to whether the data is one of split and non-split is obvious in view of the combination of the different features of Sharma. There is simply no basis in law for this line of reasoning, and furthermore, there is no basis at all in fact. Respectfully, the Appellants submit that neither the Admitted Prior Art nor Sharma, alone or in combination, suggests, let alone discloses, a serial control data signal that comprises information as to whether the data is one of split and non-split.

4. There is No Legally Sufficient Motivation to Combine the Admitted Prior Art In View of Sharma That Supports the Rejection of Claims 1, 15, 31, 46, 60, 76, 91, 106, 121, 135, 151, and 212 Under 35 U.S.C. § 103(a), and Sharma is Non-Analogous Art

It is respectfully submitted that the combination of the Admitted Prior Art and Sharma is wholly and completely improper. According to M.P.E.P. § 2143, to establish a *prima facie* case of obviousness, three basic criteria must be met. "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." [M.P.E.P. § 2143] In other words, "[o]bviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art." [M.P.E.P. § 2143.01] The Patent Office asserts that "it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the Sharma's teaching onto the prior art because Sharma teaches how to accommodate devices with either split or non-split capability." [Final Office Action, page 7] The Patent Office's stated motivation for combining Sharma with the Admitted Prior Art is completely without support in the Admitted Prior Art or in Sharma, as there is absolutely no disclosure or

suggestion in the Admitted Prior Art or in Sharma, either explicitly or implicitly, regarding the desirability for split or non-split capability.

It is respectfully submitted that there is there is absolutely no teaching, suggestion or motivation, either explicitly or implicitly, to combine the references in the manner suggested by the Patent Office. Consequently, it is respectfully submitted that the Patent Office has not established a *prima facie* case of obviousness.

It is noteworthy that the Patent Office admits in this case that "it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon *hindsight reasoning*." [Final Office Action, page 7 (emphasis added)] According to M.P.E.P. § 2142, "[t]o reach a proper determination under 35 U.S.C. 103, . . . impermissible hindsight must be avoided and the legal conclusion [of obviousness] must be reached on the basis of the facts gleaned from the prior art." Furthermore, according to M.P.E.P. § 2143.01, "[t]he mere fact that references can be . . . modified does not render the resultant combination obvious unless the prior art also suggests the desirability of [such modification]." [citing In re Mills, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990)] The Patent Office further states that such "hindsight reasoning . . . takes into account only knowledge which was within the level of ordinary skill in the art of the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper." It is respectfully submitted the Patent Office's admission forcefully illustrates that the Patent Office has indeed included knowledge gleaned from the applicant's disclosure.

Therefore, since the Patent Office has offered no proper support or motivation for combining the references, it is respectfully submitted that the rejection based on obviousness is clearly and unequivocally founded upon "knowledge gleaned only from applicant's disclosure." [*see* M.P.E.P. § 2145] Consequently, it is respectfully submitted that the rejection entails hindsight and is, therefore, improper.

Furthermore, with respect to the rejection of claims 1, 15, 31, 46, 60, 76, 91, 106, 121, 135, 151, 212, it is respectfully submitted that Sharma is non-analogous art. According to M.P.E.P. § 2141.01(a), "[i]n order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was

concerned." [M.P.E.P. § 2141.01(a) (citations omitted)] Additionally, "[w]hile Patent Office classification of references and the cross-references in the official search notes of the class definitions are some evidence of 'nonanalogy' or 'analogy' respectively, the court has found 'the similarities and differences in structure and function of the inventions to carry far greater weight." [M.P.E.P. § 2141.01(a) (citations omitted)]

Sharma relates to a cache data system. The coherent I/O system disclosed by Sharma comprises cache units configured to support DMA read requests for cacheable data. [*see* Sharma, Abstract] In contrast to Sharma, exemplary embodiments of the present invention are directed to a versatile, latency-independent interface between hardware components. Such an interface is flexible enough to support high read and write latencies of greater than one sector, a split sector format, and a second sector mark. [*see* present application, paragraph 5, page 1] Conventional technology such as iterative turbo coding, which is being introduced into modern disk drive systems, requires more processing before the data is available, which, in turn, requires R/W channels or RDCs with higher latencies. One problem is that the conventional interface used in the shorter latency systems is not capable of supporting the higher latencies. Accordingly, the latency-independent interface according to exemplary embodiments can support higher latency R/W channel or RDC designs.

Contrary to the assertions of the Patent Office, it is respectfully submitted that Sharma is not within the field of Appellants' endeavor and not reasonably pertinent to the particular problem with which the Appellants' were concerned. Additionally, it is respectfully submitted that the "structure and function" of the inventions of Sharma and the present invention are dissimilar and different. Sharma is directed to a cache data system, while the present invention is directed to a latency-independent interface between hardware components, each of the respective inventions comprising different components and devices with different functions.

Consequently, it is respectfully submitted that Sharma is non-analogous art to the present invention, and, therefore, the Patent Office has improperly relied on Sharma in its attempt to render the claims of the present application obvious.

5. Since the Patent Office's Stated Motivation for Combining Sharma With the Admitted Prior Art Is Completely Without Support In the Admitted Prior Art or in Sharma, Sharma cannot be Combined With the Admitted Prior Art to Render Independent Claims 1, 15, 31, 46, 60, 76, 91, 106, 121, 135, 151, and 212 unpatentable Under 35 U.S.C. §103(a).

It has been shown that the motivation to combine Sharma with the Admitted Prior Art is not based on anything other than impermissible hindsight reasoning. Additionally, it is respectfully submitted that the Appellants have shown that Sharma is neither in the field of the Appellants' endeavor, nor it is reasonably pertinent to the particular problem for with the inventor was concerned. Therefore, the rejection of claims 1, 15, 31, 46, 60, 76, 91, 106, 121, 135, 151, and 212 under 35 U.S.C. §103(a) is improper and should be withdrawn.

For at least the aforementioned reasons, it is respectfully submitted that the combination of the Admitted Prior Art and Sharma does not render independent claims 1, 15, 31, 46, 60, 76, 91, 106, 121, 135, 151, 212 unpatentable.

Dependent claims 357-376 variously depend from independent claims 1, 31, 46, 76, 121 and 151, and are, therefore, patentably distinguishable over the combination of the Admitted Prior Art and Sharma for at least those reasons stated above with regard to independent claims 1, 31, 46, 76, 121 and 151.

C. Rejection of Claims 2, 16, 32, 47, 61, 77, 92, 107, 122, 136, 152, and 213 Under 35 U.S.C. § 103(a) as Allegedly Being Unpatentable Over the Combination of the Admitted Prior Art In View of Sharma.

It is respectfully submitted that the combination of the Admitted Prior Art and Sharma does not disclose or suggest a latency-independent interface between first and second hardware components, comprising a serial control data circuit that transmits a serial control data signal, and a data circuit that transmits or receives data under the control of the serial control data gate signal, wherein the serial control data signal comprises information as to whether the data is one of first split, continue split, and last split.

1. The Admitted Prior Art Does Not Disclose or Suggest All of the Features of Claims 2, 16, 32, 47, 61, 77, 92, 107, 122, 136, 152, and 213.

It is respectfully submitted that the Admitted Prior Art does not disclose or suggest at least the claim feature of a serial control data signal that comprises information that the data is one of first split, continue split and last split, as recited in, for example, independent claim 2 of the present invention.

2. Sharma Does Not Disclose or Suggest All of the Features of Claims 2, 16, 32, 47, 61, 77, 92, 107, 122, 136, 152, and 213.

In complete contrast to the present invention, it is respectfully submitted that Sharma does not disclose or suggest the feature of a serial control data signal that comprises information that the data is one of first split, continue split and last split, as recited in, for example, independent claim 2 of the present application.

According to Sharma, a memory request can include a transaction identifier 146, which is a unique identifier that identifies the DMA read request and is used in a split read transaction. [*see* Sharma, column 5, lines 48-50] The tag line 156 can include a transaction identifier 172, which is the identifier of a transaction initiating the DMA read request and is used in the split read transaction. [*see* Sharma, column 6, lines 20-22] The status line 158 can

include a split read ("SR") state that means split read mode. [*see* Sharma, column 7, lines 13-15] As disclosed by Sharma,

> split read transaction is a DMA read request for data that can span one or more cache lines. In a typical split read transaction, the request is for X bytes of data relative to starting address Y. The I/O bridge unit 116 then returns X bytes of data which can span one or more cache lines. In addition, once the requesting I/O device 122 makes the DMA read request, it does not need to retry the DMA read request in the event the requested data is not resident in the cache 152 of the I/O bridge unit 116. Instead, the cache controller unit 150 returns the cache line as soon as it receives the line. [Sharma, column 8, lines 18-28]

According to Sharma, "[i]n the case of a split read transaction, the SR bit is set (i.e., SR = '1'b) and for non-split transactions, the SR bit is turned off (i.e., SR = '0'b)." [Sharma, column 9, lines 4-6]

Thus, although Sharma discloses split read transactions, it is respectfully submitted that *nowhere* does Sharma disclose or suggest a serial control data signal, particularly a serial control data signal that comprises information that the data is one of first split, *continue split* and last split, as recited in, for example, independent claim 2 of the present application.

The Patent Office proffers that because Sharma discloses an "indication for the split mode, the number of requesting bits, and a unique transaction identifier," this somehow satisfies the Appellants' request to identify where Sharma discloses or suggests such serial control data signal and such serial control data, such as a continue split. The unique transaction identifier 146 is merely a "unique identifier that identifies the DMA read request and is used in the slit read embodiment." [Sharma, column 5, lines 48-50] The unique transaction identifier 172 "is the identifier of a transaction initiating the DMA read request 130 and is used in the split read embodiment of the present invention." [Sharma, column 6, lines 20-22]

It is respectfully submitted that the Patent Office has provided absolutely no basis in fact and/or technical reasoning, absolutely no extrinsic evidence, and absolutely no support for its bald and unfounded assertion that Sharma inherently discloses a continue split according to exemplary embodiments. Rather, the Patent Office simply states that the split

read transaction disclosed by Sharma, along with the transaction identifier, somehow discloses a continue split. This assertion by the Patent Office resembles the previous unfounded assertion that "the continue split is an inherent characteristic of the split transaction to determine whether the current session is related to the previous session." [Office Action dated October 19, 2004, page 7]

Such a blatantly bald and unfounded assertion of inherency is contrary to the tenets of established patent laws and is a thoroughly improper determination of inherency. It is respectfully submitted that there is no suggestion, disclosure or teaching in Sharma to support the Patent Office's assertion of inherency, if that be the case, as Sharma does not disclose or suggest serial control data or a serial control data signal, particularly one that comprises information that the data is one of first split, continue split and last split. Rather, it is respectfully submitted that the Patent Office is basing its determination of inherency on mere "probabilities or possibilities." The Patent Office has proffered no proper evidence that makes it clear that "the missing descriptive matter is necessarily present in the thing described in the reference." Appellants respectfully traverse the assertion of inherency and request that the Patent Office cite a document in support of this determination so that the Appellants have a full and fair opportunity to respond to the combination of documents.

Therefore, it is respectfully submitted that Sharma does not address the above-identified deficiencies of the Admitted Prior Art.

3. There Is No Legally Sufficient Motivation to Combine the Admitted Prior Art In View of Sharma That Supports the Rejection of Claims 2, 16, 32, 47, 61, 77, 92, 107, 122, 136, 152, and 213 Unpatentable Under 35 U.S.C. § 103(a).

It is respectfully submitted that the Patent Office's has provided absolutely no stated motivation for combining Sharma with the Admitted Prior Art. As neither the Admitted Prior Art nor Sharma discloses or suggests numerous features of the present invention, it is respectfully submitted that there is there is no teaching, suggestion or motivation, either explicitly or implicitly, to combine the references in the manner suggested by the Patent Office. Consequently, it is respectfully submitted that the Patent Office has not established a

prima facie case of obviousness. For at least the aforementioned reasons, it is respectfully submitted that the combination of the Admitted Prior Art and Sharma does not render claims 2, 16, 32, 47, 61, 77, 92, 107, 122, 136, 152, and 213 unpatentable.

Rather, since the Patent Office has offered no proper support or motivation for combining the references, it is respectfully submitted that the rejection based on obviousness is clearly and unequivocally founded upon "knowledge gleaned only from applicant's disclosure." [*see* M.P.E.P. § 2145] Consequently, it is respectfully submitted that the rejection entails hindsight and is, therefore, improper.

For at least the foregoing reasons, it is respectfully submitted that the combination of the Admitted Prior Art and Sharma does not render the subject matter of claims 2, 16, 32, 47, 61, 77, 92, 107, 122, 136, 152, and 213 unpatentable. Accordingly, reconsideration and withdrawal of these grounds of rejection are respectfully requested.

4. Since Sharma Does Not Disclose All the Features of Appellants' Claimed Invention, and the Patent Office has Not Provided Legally Sufficient Motivation To Combine the Admitted Prior Art with Sharma, the Combination of Sharma and the Admitted Prior Art Cannot Render Claims 2, 16, 32, 47, 61, 77, 92, 107, 122, 136, 152, and 213 Unpatentable Under 35 U.S.C. §103(a).

The Appellants have shown the Sharma does not teach or suggest the claimed feature of the serial control data signal comprising information that the data is one of a first split, continue split, and last split. The Appellants have further shown that the feature of the serial control data signal comprising information that the data is one of a fist split, continue split, and last split is also not inherent in the Sharma patent, and that the combination of features taught by Sharma does not, in any manner whatsoever, teach or suggest the claimed feature of Appellants' invention. In regard to rejections made under 35 U.S.C. §103(a), it is well known that to establish a *prima facie* case of obviousness, the prior art must disclose or suggest all of the limitations of the claims. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). Therefore, as In re Royka teaches, a *prima facie* case of obviousness has not been made, and therefore it is respectfully submitted that the aforementioned claims are allowable over the prior art. Further, it has been shown that the motivation to combine the

Sharma patent with the Admitted Prior Art is not based on anything other than impermissible hindsight reasoning. Therefore, the rejection of claims 2, 16, 32, 47, 61, 77, 92, 107, 122, 136, 152, and 213 as unpatentable under 35 U.S.C. §103(a) is improper and should be withdrawn.

For at least the aforementioned reasons, it is respectfully submitted that the combination of the Admitted Prior Art and Sharma does not render independent claims 2, 16, 32, 47, 61, 77, 92, 107, 122, 136, 152, and 213 unpatentable.

Dependent claims 3, 4, 7, 9-11, 17, 18, 21, 23-25, 33, 34, 37-41, 48, 49, 52, 54-56, 62, 63, 66, 68-70, 78, 79, 82, 84-86, 93, 94, 97, 99-101, 108, 109, 112, 114-116, 123, 124, 127, 129-131, 137, 138, 141, 143-145, 153, 154, 157, 159-161, 214, 215, 218, and 220-222 variously depend from independent claims 2, 16, 32, 47, 61, 77, 92, 107, 122, 136, 152, and 213, and are, therefore, patentably distinguishable over the combination of the Admitted Prior Art and Sharma for at least those reasons stated above with regard to independent claims 2, 16, 32, 47, 61, 77, 92, 107, 122, 136, 152, and 213.

Hence, the subject matter of these claims is separately patentable for this reason.

D. Rejection of Claims 6, 20, 36, 51, 65, 81, 96, 111, 126, 140, 156, and 217 Under 35 U.S.C. §103(a) as Allegedly Being Unpatentable Over the Combination of the Admitted Prior Art In View of Sharma.

It is respectfully submitted that the combination of the Admitted Prior Art and Sharma does not disclose or suggest a latency-independent interface between first and second hardware components, comprising a serial control data circuit that transmits a serial control data signal, and a data circuit that transmits or receives data under the control of the serial control data gate signal, wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

1. The Admitted Prior Art Does Not Disclose or Suggest All of the Features of Claims 6, 20, 36, 51, 65, 81, 96, 111, 126, 140, 156, and 217.

The Admitted Prior Art does not disclose or suggest at least the claim feature of a serial control data signal that comprises information if a succeeding serial control data is a continuation of a current serial control data.

2. Sharma Does Not Disclose or Suggest All of the Features of Claims 6, 20, 36, 51, 65, 81, 96, 111, 126, 140, 156, and 217.

Even if one were to combine the Admitted Prior Art with Sharma, in the manner suggested by the Patent Office, the rejection of claims 6, 20, 36, 51, 65, 81, 96, 111, 126, 140, 156, and 217 is still improper, because the proposed combination of references does not disclose all of the features of the aforementioned claims.

Simply put, the Patent Office has made *no attempt* to show where Sharma discloses or suggests the claim feature of a serial control data signal comprising information if a succeeding serial control data is a continuation of a current serial control data.

3. There Is No Legally Sufficient Motivation To Combine the Admitted Prior Art In View of Sharma That supports the Rejection of Claims 6, 20, 36, 51, 65, 81, 96, 111, 126, 140, 156, and 217 Under 35 U.S.C. §103(a).

To establish a *prima facie* case of obviousness, the Patent Office must show that "some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead [an]individual to combine the relevant teachings of the references." In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). "The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). The showing must be "clear and particular, and it must be supported by actual evidence." Teleflex, Inc. v. Ficosa North American Corp., 299 F.3d 1313, 1334, 63 U.S.P.Q.2d 1374, 1387 (Fed. Cir. 2002) (quoting In re Dembiczak, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999)). It is not sufficient to rely on "common sense and common knowledge," there must be specific evidence to support the motivation. *See* In re Lee, 277 F.3d. 1338, 1344-45, 61 U.S.P.Q.2d 1430, 1434-35 (Fed. Cir. 2002).

In this case, the Patent Office has made no showing, *whatsoever*, of a motivation to combine based on actual, specific evidence.

4. Since Neither the Admitted Prior Art Nor Sharma Disclose All of the Features of Appellants' Claimed Invention, and the Patent Office has Not Provided Legally Sufficient Motivation To Combine the Admitted Prior Art with Sharma, the Combination of Sharma and the Admitted Prior Art Cannot Render Claims 6, 20, 36, 51, 65, 81, 96, 111, 126, 140, 156, and 217 Unpatentable Under 35 U.S.C. §103(a).

The Patent Office has not shown where the Admitted Prior Art or Sharma discloses or suggests the claimed feature of the serial control data signal comprising information if a succeeding serial control data is a continuation of a current serial control data taught or suggested. Furthermore, the Patent Office has failed to provide any legally sufficient motivation to combine Sharma and the Admitted Prior Art. Therefore, it is respectfully submitted that the Patent Office has failed to make a *prima facie* case under 35 U.S.C.

§103(a), and, therefore, claims 6, 20, 36, 51, 65, 81, 96, 111, 126, 140, 156, and 217 are allowable over the prior art. Therefore, the rejection of claims 6, 20, 36, 51, 65, 81, 96, 111, 126, 140, 156, and 217 as allegedly unpatentable under 35 U.S.C. §103(a) is improper and should be withdrawn.

For at least the aforementioned reasons, it is respectfully submitted that the combination of the Admitted Prior Art and Sharma does not render independent claims 6, 20, 36, 51, 65, 81, 96, 111, 126, 140, 156, and 217 unpatentable.

Dependent claims 255-260, 273-278, 291-296, 309-314, 327-332, and 345-350 variously depend from independent claims 6, 20, 36, 51, 65, 81, 96, 111, 126, 140, 156, and 217, and are, therefore, patentably distinguishable over the combination of the Admitted Prior Art and Sharma for at least those reasons stated above with regard to independent claims 6, 20, 36, 51, 65, 81, 96, 111, 126, 140, 156, and 217.

Hence, the subject matter of these claims is separately patentable for this reason.

E. Rejection of Claims 9, 23, 39, 54, 68, 84, 99, 114, 129, 143, 159, 220, 252, 258, 264, 270, 276, 282, 288, 294, 300, 306, 312, 318, 324, 330, 336, 342, 348, 354, 360, and 366 Under 35 U.S.C. §103(a) as Allegedly Being Unpatentable Over the Combination of the Admitted Prior Art In View of Sharma.

1. There Is No Legally Sufficient Motivation To Combine The Admitted Prior Art In View Of Sharma That Supports the Rejection of Claims 9, 23, 39, 54, 68, 84, 99, 114, 129, 143, 159, 220, 252, 258, 264, 270, 276, 282, 288, 294, 300, 306, 312, 318, 324, 330, 336, 342, 348, 354, 360, and 366 Under 35 U.S.C. §103(a).

Based on the requirements set forth above, there is no motivation to combine the admitted prior art in view of Sharma that supports the rejection of claims 9, 23, 39, 54, 68, 84, 99, 114, 129, 143, 159, 220, 252, 258, 264, 270, 276, 282, 288, 294, 300, 306, 312, 318, 324, 330, 336, 342, 348, 354, 360, and 366 Under 35 U.S.C. §103(a). In this case, the Patent Office has made no showing, *whatsoever*, of a motivation to combine based on actual, specific evidence. Indeed, the Patent Office has failed to make any showing of a motivation based on actual, specific evidence to combine the Admitted Prior Art and Sharma. Therefore, the Patent Office has failed to make a *prima facie* case of obviousness, and it is respectfully submitted that claims 9, 23, 39, 54, 68, 84, 99, 114, 129, 143, 159, 220, 252, 258, 264, 270, 276, 282, 288, 294, 300, 306, 312, 318, 324, 330, 336, 342, 348, 354, 360, and 366 are allowable over the Admitted Prior Art and Sharma.

2. Since the Patent Office Has Not Provided Legally Sufficient Motivation To Combine the Admitted Prior Art with Sharma, the Combination of Sharma and the Admitted Prior Art Cannot Render Claims 6, 20, 36, 51, 65, 81, 96, 111, 126, 140, 156, and 217 Unpatentable Under 35 U.S.C. §103(a).

The Patent Office has failed to make any showing of a motivation based on actual, specific evidence to combine the Admitted Prior Art and Sharma. Therefore, the Patent Office has failed to make a *prima facie* case of obviousness, and it is respectfully submitted that claims 9, 23, 39, 54, 68, 84, 99, 114, 129, 143, 159, 220, 252, 258, 264, 270, 276, 282,

288, 294, 300, 306, 312, 318, 324, 330, 336, 342, 348, 354, 360, and 366 are allowable over the Admitted Prior Art and Sharma. Therefore, the rejection of claims 9, 23, 39, 54, 68, 84, 99, 114, 129, 143, 159, 220, 252, 258, 264, 270, 276, 282, 288, 294, 300, 306, 312, 318, 324, 330, 336, 342, 348, 354, 360, and 366 as allegedly being unpatentable under 35 U.S.C. §103(a) is improper and should be withdrawn.

For at least the aforementioned reasons, it is respectfully submitted that the combination of the Admitted Prior Art and Sharma does not render claims 9, 23, 39, 54, 68, 84, 99, 114, 129, 143, 159, 220, 252, 258, 264, 270, 276, 282, 288, 294, 300, 306, 312, 318, 324, 330, 336, 342, 348, 354, 360, and 366 unpatentable.

Hence, the subject matter of these claims is separately patentable for this reason.

F. Rejection of Claims 3, 4, 17, 18, 33, 34, 48, 49, 62, 63, 78, 79, 93, 94, 108, 109, 123, 124, 137, 138, 153, 154, 214, 215, 249, 250, 255, 256, 261, 262, 267, 268, 276, 274, 279, 280, 285, 286, 291, 292, 297, 298, 303, 304, 309, 310, 315, 316, 321, 322, 327, 328, 333, 334, 339, 340, 345, 346, 351, 352, 357, 358, 363, 364, 369, 371, 373, and 375 Under 35 U.S.C. § 103(a) as Allegedly Being Unpatentable Over the Combination of the Admitted Prior Art In View of Dunn.

It is respectfully submitted that the combination of the Admitted Prior Art and Dunn does not disclose or suggest a latency-independent interface between first and second hardware components, comprising a serial control data circuit that transmits a serial control data signal, and a data circuit that transmits or receives data under the control of the serial control data gate signal, wherein the serial control data signal comprises an amount of data to be written during a write operation, or an amount of data to be read during a read operation.

As a preliminary matter, the Patent Office neglected to discuss claims 49, 63, 79, 94, 109, 124, 138, 154, and 215, as these claims recite the feature of the serial data control signal comprising an amount of the data to be read during a read operation. The Appellants presume this was an oversight by the Patent Office, and includes these claims in the present discussion as if the Patent Office had listed them with other similar claims.

1. The Dunn Patent.

As understood by the Appellants, Dunn is directed towards a data processing system in which information bearing signals are recorded in one of a plurality of record formats on one record medium. The format selected can be commanded or based upon record lengths, in bytes. When the record length equals or exceeds a predetermined number of bytes, then one record is recorded in each signal block of the record format. When the record length is less than the predetermined number, then a second format is used which inserts several of the records in one of the signal blocks. The signal block and its packets respectively contain indications of formats such that any one of several formats can be used on one record medium and in one signal block having a plurality of variable length packets. Logical

indicators, such as format marks, tape marks, and the like, can separate formats used on the storage medium. [*see* Dunn, Abstract]

2. The Admitted Prior Art Does Not Disclose or Suggest All the Claim Features of Claims 3, 4, 17, 18, 33, 34, 48, 49, 62, 63, 78, 79, 93, 94, 108, 109, 123, 124, 137, 138, 153, 154, 214, 215, 249, 250, 255, 256, 261, 262, 267, 268, 276, 274, 279, 280, 285, 286, 291, 292, 297, 298, 303, 304, 309, 310, 315, 316, 321, 322, 327, 328, 333, 334, 339, 340, 345, 346, 351, 352, 357, 358, 363, 364, 369, 371, 373, and 375.

The Patent Office admits that "[t]he [admitted] prior art does not explicitly disclose specifying the amount of the data or codeword in each session is a common practice in constructing data packets." [Final Office Action, page 4] Thus, although it is not clear to the Appellants what point the Patent Office is intending to make by baldly alleging what may be "common practice," it is respectfully submitted that it is entirely clear that the Patent Office has acknowledged that the Admitted Prior Art does not disclose or suggest the feature of a serial control data signal that comprises an amount of data to be written during a write operation, or an amount of data to be read during a read operation.

3. Dunn Does Not Disclose or Suggest All of the Features of Claims 3, 4, 17, 18, 33, 34, 48, 49, 62, 63, 78, 79, 93, 94, 108, 109, 123, 124, 137, 138, 153, 154, 214, 215, 249, 250, 255, 256, 261, 262, 267, 268, 276, 274, 279, 280, 285, 286, 291, 292, 297, 298, 303, 304, 309, 310, 315, 316, 321, 322, 327, 328, 333, 334, 339, 340, 345, 346, 351, 352, 357, 358, 363, 364, 369, 371, 373, and 375.

Even if one were to combine the Admitted Prior Art with the Dunn reference, as suggested by the Patent Office, the rejection of the claims is still improper because the proposed combination of references does not disclose all of the features of the aforementioned claims.

Simply put, the Patent Office has made *no attempt* to show where Dunn discloses or suggests the claim feature of a serial control data signal comprising an amount of data to be written during a write operation, or an amount of data to be read during a read operation.

4. There Is No Legally Sufficient Motivation To Combine The Admitted Prior Art In View Dunn That Supports the Rejection of Claims 3, 4, 17, 18, 33, 34, 48, 49, 62, 63, 78, 79, 93, 94, 108, 109, 123, 124, 137, 138, 153, 154, 214, 215, 249, 250, 255, 256, 261, 262, 267, 268, 276, 274, 279, 280, 285, 286, 291, 292, 297, 298, 303, 304, 309, 310, 315, 316, 321, 322, 327, 328, 333, 334, 339, 340, 345, 346, 351, 352, 357, 358, 363, 364, 369, 371, 373, and 375 Under 35 U.S.C. § 103(a).

Based on the requirements set forth above, there is no legally sufficient motivation to combine the Admitted Prior Art in view of Dunn that supports the rejection of claims 3, 4, 17, 18, 33, 34, 48, 49, 62, 63, 78, 79, 93, 94, 108, 109, 123, 124, 137, 138, 153, 154, 214, 215, 249, 250, 255, 256, 261, 262, 267, 268, 276, 274, 279, 280, 285, 286, 291, 292, 297, 298, 303, 304, 309, 310, 315, 316, 321, 322, 327, 328, 333, 334, 339, 340, 345, 346, 351, 352, 357, 358, 363, 364, 369, 371, 373, and 375 under 35 U.S.C. § 103(a).

In this case, the Patent Office has made no showing, *whatsoever*, of a motivation to combine based on actual, specific evidence. *Even if* one were to combine the Admitted Prior Art with the Dunn reference, as suggested by the Patent Office, the rejection of the claims is still improper because the proposed combination of references does not disclose all of the features of the aforementioned claims.

Simply put, the Patent Office has made no attempt to show where the prior art discloses or suggests the claimed feature of a serial control data signal comprising an amount of data to be written during a write operation, or an amount of data to be read during a read operation.

5. Since Neither the Admitted Prior Art nor Dunn Discloses or Suggests All of the Features of Appellants' Claimed Invention, and the Patent Office has Not Provided Legally Sufficient Motivation To Combine the Admitted Prior Art with Dunn, the Combination of Dunn and the Admitted Prior Art Cannot Render Claims 3, 4, 17, 18, 33, 34, 48, 49, 62, 63, 78, 79, 93, 94, 108, 109, 123, 124, 137, 138, 153, 154, 214, 215, 249, 250, 255, 256, 261, 262, 267, 268, 276, 274, 279, 280, 285, 286, 291, 292, 297, 298, 303, 304, 309, 310, 315, 316, 321, 322, 327, 328, 333, 334, 339, 340, 345, 346, 351, 352, 357, 358, 363, 364, 369, 371, 373, and 375 Unpatentable Under 35 U.S.C. §103(a).

The Patent Office has not shown where the Admitted Prior Art or Dunn discloses or suggests the claimed feature of the serial control data signal comprising an amount of data to be written during a write operation or an amount of data to be read during a read operation taught or suggested. Furthermore, the Patent Office has failed to provide any legally sufficient motivation to combine Dunn and the Admitted Prior Art. Therefore, it is respectfully submitted that the Patent Office has failed to make a *prima facie* case under 35 U.S.C. §103(a), and thus, claims 3, 4, 17, 18, 33, 34, 48, 49, 62, 63, 78, 79, 93, 94, 108, 109, 123, 124, 137, 138, 153, 154, 214, 215, 249, 250, 255, 256, 261, 262, 267, 268, 276, 274, 279, 280, 285, 286, 291, 292, 297, 298, 303, 304, 309, 310, 315, 316, 321, 322, 327, 328, 333, 334, 339, 340, 345, 346, 351, 352, 357, 358, 363, 364, 369, 371, 373, and 375 are allowable over the prior art. Therefore, the rejection of claims 93, 4, 17, 18, 33, 34, 48, 49, 62, 63, 78, 79, 93, 94, 108, 109, 123, 124, 137, 138, 153, 154, 214, 215, 249, 250, 255, 256, 261, 262, 267, 268, 276, 274, 279, 280, 285, 286, 291, 292, 297, 298, 303, 304, 309, 310, 315, 316, 321, 322, 327, 328, 333, 334, 339, 340, 345, 346, 351, 352, 357, 358, 363, 364, 369, 371, 373, and 375 as allegedly being unpatentable under 35 U.S.C. §103(a) is improper and should be withdrawn.

For at least the aforementioned reasons, it is respectfully submitted that the combination of the Admitted Prior Art and Dunn does not render claims 3, 4, 17, 18, 33, 34, 48, 49, 62, 63, 78, 79, 93, 94, 108, 109, 123, 124, 137, 138, 153, 154, 214, 215, 249, 250, 255, 256, 261, 262, 267, 268, 276, 274, 279, 280, 285, 286, 291, 292, 297, 298, 303, 304, 309, 310, 315, 316, 321, 322, 327, 328, 333, 334, 339, 340, 345, 346, 351, 352, 357, 358, 363, 364, 369, 371, 373, and 375 unpatentable.

Hence, the subject matter of these claims is separately patentable for this reason.

G. Rejection of Claims 5, 19, 35, 50, 64, 80, 95, 110, 125, 139, 155, and 216 Under 35 U.S.C. § 103(a) as Allegedly Being Unpatentable Over the Combination of the Admitted Prior Art In View of Dunn.

It is respectfully submitted that the combination of the Admitted Prior Art and Dunn does not disclose or suggest a latency-independent interface between first and second hardware components, comprising a serial control data circuit that transmits a serial control data signal, and a data circuit that transmits or receives data under the control of the serial control data gate signal, wherein the serial control data signal comprises a codeword size of a current sector.

1. The Admitted Prior Art Does Not Disclose or Suggest All of the Features of Claims 5, 19, 35, 50, 64, 80, 95, 110, 125, 139, 155, and 216.

The Patent Office admits that "[t]he [admitted] prior art does not explicitly disclose specifying the amount of the data or codeword in each session is a common practice in constructing data packets." [Final Office Action, page 4] Thus, it is respectfully noted that the Patent Office has acknowledged that the Admitted Prior Art does not disclose or suggest the feature of a serial control data signal that comprises a codeword size of a current sector, without regard as to whether it is a common practice or not.

2. Dunn Does Not Disclose or Suggest All of the Features of Claims 5, 19, 35, 50, 64, 80, 95, 110, 125, 139, 155, and 216.

Even if one were to combine the Admitted Prior Art with Dunn, as suggested by the Patent Office, the rejection of the claims is still improper, because the proposed combination of references does not disclose or suggest all of the features of the aforementioned claims. In particular, it is respectfully submitted that Dunn does not disclose or suggest that feature of a serial control data signal that comprises a codeword size of a current sector, without regard as to whether it is a common practice or not.

The Patent Office states that "PCT CNT [sic; presumably, the Patent Office meant "PKT CNT"] indicates the number of packets in the block . . . [and] is equivalent to the claimed code word size of the current sector." While it may be true that PKT CNT does reflect the number of packets in the block, the Patent Office utterly fails to explain how it arrives at its conclusion of "equivalence." It is respectfully noted that the number of packets is *not* the same as the codeword size of a current sector.

3. There is No Legally Sufficient Motivation to Combine the Admitted Prior Art In View of Dunn That Supports the Rejection of Claims 5, 19, 35, 50, 64, 80, 95, 110, 125, 139, 155, and 216 Under 35 U.S.C. § 103(a).

Based on the requirements set forth above, there is no legally sufficient motivation to combine the Admitted Prior Art in view of Dunn that supports the rejection of claims 5, 19, 35, 50, 64, 80, 95, 110, 125, 139, 155, and 216 under 35 U.S.C. § 103(a). In this case, the Patent Office has made no showing of a motivation to combine based on actual evidence. With respect to the combination of Dunn and the Admitted Prior Art, the Patent Office asserts that it "would have been obvious to one having ordinary skill in the computer art at the time Appellants made the invention to adapt Dunn's teaching into the prior art because Dunn enables one to improve transmission efficiency by controlling the data amount in each sessions." [*see* Final Office Action, April 20, 2005, page 4] The Patent Office cites no evidence in support of this purported motivation. Neither the Admitted Prior Art nor Dunn suggests that transmission efficiency can be improved by controlling the data amount in each sessions. Furthermore, the Patent Office appears to be suggesting that because Dunn "enables one to improve the transmission efficiency by controlling the data amount in each session," this is a motivation to combine the Admitted Prior Art and Dunn. This is simply not the case. The Patent Office has not suggested a motivation for combining the Admitted Prior Art and Dunn, as much as the Patent Office has cited presumed and unsupported benefits of the Dunn patent. It is noted that the claims recite that "the serial control data signal comprises a codeword size of a current sector." The motivation provided by the Patent Office is simply a naked assertion, completely unsupported by any actual evidence.

The simple fact is that the Patent Office has collected random pieces of prior art showing various bits and pieces of the Appellants' invention, and created motivations out of whole cloth to support combining the random pieces of prior art. This is simply impermissible. Because the Patent Office has not identified a motivation to combine which is supported by actual, specific evidence, the Patent Office has failed to establish a *prima facie* case of obviousness.

4. Since the Patent Office Has Not Provided Legally Sufficient Motivation To Combine the Admitted Prior Art with Dunn, Nor has the Patent Office Shown that the Admitted Prior Art and Dunn Teach or Suggest all the Claim Features, the Combination of Dunn and the Admitted Prior Art Cannot Render Claims 5, 19, 35, 50, 64, 80, 95, 110, 125, 139, 155, and 216 Unpatentable Under 35 U.S.C. §103(a).

The Patent Office has failed to make any showing of a motivation based on actual, specific evidence to combine the Admitted Prior Art and Dunn. Furthermore, the Patent Office has failed to show that the Admitted Prior Art and Dunn teaches or suggests the claim feature of a serial control data signal comprising a codeword size of a current sector. Therefore, the Patent Office has failed to make a *prima facie* case of obviousness, and it is respectfully submitted that claims 5, 19, 35, 50, 64, 80, 95, 110, 125, 139, 155, and 216 are allowable over the Admitted Prior Art and Dunn. Therefore, the rejection of claims 5, 19, 35, 50, 64, 80, 95, 110, 125, 139, 155, and 216 as allegedly being unpatentable under 35 U.S.C. §103(a) is improper and should be withdrawn.

For at least the aforementioned reasons, it is respectfully submitted that the combination of the Admitted Prior Art and Dunn does not render independent claims 5, 19, 35, 50, 64, 80, 95, 110, 125, 139, 155, and 216 unpatentable.

Dependent claims 249, 250, 251-254, 267-272, 285-290, 303-308, 321-326, and 339-344 variously depend from independent claims 5, 19, 35, 50, 64, 80, 95, 110, 125, 139, 155, and 216, and are, therefore, patentably distinguishable over the combination of the Admitted Prior Art and Sharma for at least those reasons stated above with regard to independent claims 6, 20, 36, 51, 65, 81, 96, 111, 126, 140, 156, and 217.

Hence, the subject matter of these claims is separately patentable for this reason.

H. Rejection of Claims 8, 22, 38, 53, 67, 83, 98, 113, 128, 142, 158, and 219 Under 35 U.S.C. § 103(a) as Allegedly Being Unpatentable Over the Combination of the Admitted Prior Art In View of Dunn.

It is respectfully submitted that the combination of the Admitted Prior Art and Dunn does not disclose or suggest a latency-independent interface between first and second hardware components, comprising a serial control data circuit that transmits a serial control data signal, and a data circuit that transmits or receives data under the control of the serial control data gate signal, wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and further comprises a ready transceiver that transmits or receives a bi-directional ready signal.

1. The Admitted Prior Art Does Not Disclose or Suggest All the Claim Features of Claims 8, 22, 38, 53, 67, 83, 98, 113, 128, 142, 158, and 219.

The Patent Office admits that "[t]he [admitted] prior art does not explicitly disclose claim [sic; presumably, the Patent Office meant to say "disclose," or words to that effect] a ready signal." [Final Office Action, page 5] Furthermore, the Patent Office then states that "Dunn discloses the ready status/signal when the operation related contingence met [sic]." [Final Office Action, page 5] At least implicitly, therefore, the Patent Office admits that the Admitted Prior Art also does not disclose or suggest a ready transceiver that transmits or receives a bi-directional ready signal.

2. Dunn Does Not Disclose or Suggest All the Claim Features of Claims 8, 22, 38, 53, 67, 83, 98, 113, 128, 142, 158, and 219.

Even if one were to combine the Admitted Prior Art with Dunn, as suggested by the Patent Office, the rejection of the claims is still improper, because the proposed combination of references does not disclose all of the features of the aforementioned claims. In particular, it is respectfully submitted that Dunn does not disclose or suggest the feature of a ready transceiver that transmits or receives a bi-directional ready signal.

The Patent Office states that "Dunn discloses a status store for storing/monitoring status for the data processing operations (column 15, lines 40-16); thus Dunn discloses the ready status/signal when the operation related contingence met [sic]." [Final Office Action, April 20, 2005, page 5] Respectfully, the Patent Office has failed to appreciate the difference between a "ready signal" and a "ready transceiver."

Dunn discloses that "[e]ach of the status stores 300 contain a plurality of registers for containing bits relating to device status, buffer status, channel status, and the like. Such status information reflects the selection status of the device, its busy status, contingent connections and all other status necessary for operating the storage subsystem with the input/output channel 214." [Dunn, column 15, lines 40-47] In particular, Dunn discloses that

> [s]tatus stores 300 also communicate with the respective channel adaptors in the control units 11 via cables 303. Such communication includes the supplying of device busy status to the channel adaptors from the status stores and the request for selection from the channel adaptors to the status stores; that is, if CAB 280 wants to select device D6 on behalf of a host request, CAB 280 communicates with its status store 300 of CU-0 requesting that the device D6 be selected. Status store 300 will supply the busy or not busy status of D6 to CAB. CAB then immediately responds to the host request with respect to device D6, thereby reducing selection and inquiry time between a host 212 and control units 211. [Dunn, column 15, line 61 – column 16, line 6]

Dunn discloses that the status stores 300 supply the busy or not busy status and that the status stores 300 are comprised of a plurality of registers. It is respectfully submitted that *nowhere* does Dunn disclose or suggest the feature of a ready transceiver that transmits or receives a bi-directional ready signal. It is respectfully noted that the Patent Office has failed to point out, in any previous Office Action or the during the previously held interview, where Dunn discloses such a ready transceiver.

3. There is No Legally Sufficient Motivation to Combine the Admitted Prior Art in View of Dunn That Supports the Rejection of Claims 8, 22, 38, 53, 67, 83, 98, 113, 128, 142, 158, and 219 Under 35 U.S.C. § 103(a).

Based on the requirements set forth above, there is no legally sufficient motivation to combine the Admitted Prior Art in view of Dunn that supports the rejection of claims 8, 22, 38, 53, 67, 83, 98, 113, 128, 142, 158, and 219 under 35 U.S.C. § 103(a). In this case, the Patent Office has made no showing, *whatsoever*, of a motivation to combine based on actual, specific evidence. Because the Patent Office has not identified a motivation to combine which is supported by actual, specific evidence, the Patent Office has failed to establish a *prima facie* case of obviousness.

4. Since the Patent Office Has Not Provided Legally Sufficient Motivation To Combine the Admitted Prior Art with Dunn, Nor has the Patent Office Shown that the Admitted Prior Art and Dunn Teaches or Suggests all the Claim Features, the Combination of Dunn and the Admitted Prior Art Cannot Render Claims 8, 22, 38, 53, 67, 83, 98, 113, 128, 142, 158, and 219 Unpatentable Under 35 U.S.C. §103(a).

The Patent Office has failed to make any showing of a motivation based on actual, specific evidence to combine the Admitted Prior Art and Dunn. Furthermore, the Patent Office has failed to show that the combination of the Admitted Prior Art and Dunn teaches or suggests the claim feature of a ready transceiver that transmits or receives a bi-directional ready signal. Therefore, the Patent Office has failed to make a *prima facie* case of obviousness, and it is respectfully submitted that claims 8, 22, 38, 53, 67, 83, 98, 113, 128, 142, 158, and 219 are allowable over the Admitted Prior Art and Dunn. Therefore, the rejection of claims 8, 22, 38, 53, 67, 83, 98, 113, 128, 142, 158, and 219 as allegedly being unpatentable under 35 U.S.C. §103(a) is improper and should be withdrawn.

For at least the aforementioned reasons, it is respectfully submitted that the combination of the Admitted Prior Art and Dunn does not render independent claims 8, 22, 38, 53, 67, 83, 98, 113, 128, 142, 158, and 219 unpatentable.

Dependent claims 261-266, 279-284, 297-302, 315-320, 333-338, and 351-356 variously depend from independent claims 8, 22, 38, 53, 67, 83, 98, 113, 128, 142, 158, and

219, and are, therefore, patentably distinguishable over the combination of the Admitted Prior Art and Sharma for at least those reasons stated above with regard to independent claims 8, 22, 38, 53, 67, 83, 98, 113, 128, 142, 158, and 219.

Hence, the subject matter of these claims is separately patentable for this reason.

I. Rejection of Claims 7, 21, 37, 52, 66, 82, 97, 112, 127, 141, 157, 218 10, 24, 40, 55, 69, 85,100, 115, 130, 144, 160, 221 11, 25, 41, 56, 70, 86, 101, 116, 131, 145, 161, 222, 215, 253, 254, 257, 259, 260, 263, 265, 266, 271, 272, 275, 277, 278, 281, 283, 284, 287, 289, 290, 293, 295, 296, 299, 301, 302, 305, 307, 308, 311, 313, 314, 317, 319, 320, 323, 325, 326, 329, 331, 332, 336, 337, 338, 341, 343, 344, 347, 349, 350, 353, 355, 356 ,359 ,361, 362, 365, 367, 368, 370, 372, 374, and 376 Under 35 U.S.C. § 103(a) as Allegedly Being Unpatentable Over the Combination of the Admitted Prior Art In View of Dunn, further in view of Bliss et al. (U.S. Patent No. 6,009,549, hereinafter "Bliss").

It is respectfully submitted that the Admitted Prior Art, Dunn and Bliss, alone or in combination, do not disclose a latency-independent interface between first and second hardware components, comprising, a serial control data circuit that transmits a serial control data signal, and a data circuit that transmits or receives data under the control of the serial control data signal, wherein the serial control data signal comprises during a write operation information as to a start of a sync mark and a start of write padding data, and during a read operation information that a sync mark was detected.

1. The Bliss Patent.

As understood by the Appellants, Bliss is directed towards a disk storage system wherein user data received from a host system is first encoded according to a first channel code having a high code rate, and then encoded according to an ECC code, such as a Reed-Solomon code, wherein the ECC redundancy symbols are encoded according to a second channel code having low error propagation. In Bliss, the first channel code is an RLL (d,k) code having a long k constraint that allows for longer block lengths (and higher code rates). During read back, a synchronous read channel samples the analog read signal asynchronously and interpolates the asynchronous sample values to generate sample values substantially synchronized to the baud rate. Bliss further discloses a trellis sequence detector that detects an estimated binary sequence from the synchronous sample values, wherein a state transition diagram of the trellis detector is configured according to the code constraints of the first and

second channel codes. The estimated binary sequence output by the sequence detector is buffered in a data buffer to facilitate the error detection and correction process, and to allow for retroactive and split-segment symbol synchronization using multiple sync marks. [Bliss, abstract]

2. The Admitted Prior Art Does Not Disclose or Suggest All the Claim Features of Claims 7, 21, 37, 52, 66, 82, 97, 112, 127, 141, 157, 218 10, 24, 40, 55, 69, 85,100, 115, 130, 144, 160, 221 11, 25, 41, 56, 70, 86, 101, 116, 131, 145, 161, 222, 215, 253, 254, 257, 259, 260, 263, 265, 266, 271, 272, 275, 277, 278, 281, 283, 284, 287, 289, 290, 293, 295, 296, 299, 301, 302, 305, 307, 308, 311, 313, 314, 317, 319, 320, 323, 325, 326, 329, 331, 332, 336, 337, 338, 341, 343, 344, 347, 349, 350, 353, 355, 356 ,359 ,361, 362, 365, 367, 368, 370, 372, 374, and 376.

The Patent Office admits that "[t]he [admitted] prior art does not explicitly disclose the padding data and sync mark." [Final Office Action, page 5] Thus, the Patent Office acknowledges that the Admitted Prior Art does not disclose or suggest the feature of a serial control data signal that comprises during a write operation information as to a start of a sync mark and a start of write padding data, and during a read operation information that a sync mark was detected

3. Dunn and Bliss Do Not Disclose or Suggest All the Claim Features of Claims 7, 21, 37, 52, 66, 82, 97, 112, 127, 141, 157, 218 10, 24, 40, 55, 69, 85,100, 115, 130, 144, 160, 221 11, 25, 41, 56, 70, 86, 101, 116, 131, 145, 161, 222, 215, 253, 254, 257, 259, 260, 263, 265, 266, 271, 272, 275, 277, 278, 281, 283, 284, 287, 289, 290, 293, 295, 296, 299, 301, 302, 305, 307, 308, 311, 313, 314, 317, 319, 320, 323, 325, 326, 329, 331, 332, 336, 337, 338, 341, 343, 344, 347, 349, 350, 353, 355, 356 ,359 ,361, 362, 365, 367, 368, 370, 372, 374, and 376.

Even if one were to combine the Admitted Prior Art with Bliss and Dunn, as suggested by the Patent Office, the rejection of the claims is still improper because the proposed combination of references does not disclose all of the features of the aforementioned claims. In particular, it is respectfully submitted that neither Dunn nor Bliss disclose or suggest the feature of a serial control data signal that comprises during a write

operation information as to a start of a sync mark and a start of write padding data, and during a read operation information that a sync mark was detected.

The Patent Office states that "Dunn discloses that the padding data is a known practice to align packet fields . . . so each packet is in a proper determined format. Bliss discloses the sync mark is a practice for synchronizing data stream . . ." [Final Office Action, April 20, 2005, page 5] While it may be true that the padding data is a known practice to align packet fields so that each packet is in a proper determined format, and that Bliss discloses the sync mark is a practice for synchronizing data stream, the Patent Office has completely and utterly failed to show how these assertions meets the claimed feature of a serial control data signal comprising during a write operation information as to a start of a sync mark and a start of a write padding data, and during a read operation information that a sync mark was detected.

Furthermore, the Patent Office asserts that Bliss teaches the sync transceiver as recited in dependent claims 10, 24, 40, 55, 69, 85, 100, 115, 130, 144, 160 and 221. This is simply not the case. The Patent Office cites Figure 4, structure 4 of Bliss in support of such an assertion. However, upon inspection, such a citation merely reveals a sync *detector*.

4. There is No Legally Sufficient Motivation to Combine the Admitted Prior Art In View of Dun and Further In View of Bliss That Supports the Rejection of Claims 7, 21, 37, 52, 66, 82, 97, 112, 127, 141, 157, 218, 10, 24, 40, 55, 69, 85,100, 115, 130, 144, 160, 221 11, 25, 41, 56, 70, 86, 101, 116, 131, 145, 161, 222, 215, 253, 254, 257, 259, 260, 263, 265, 266, 271, 272, 275, 277, 278, 281, 283, 284, 287, 289, 290, 293, 295, 296, 299, 301, 302, 305, 307, 308, 311, 313, 314, 317, 319, 320, 323, 325, 326, 329, 331, 332, 336, 337, 338, 341, 343, 344, 347, 349, 350, 353, 355, 356 ,359 ,361, 362, 365, 367, 368, 370, 372, 374, and 376 Under 35 U.S.C. §103(a).

Based on the requirements set forth above, there is no legally sufficient motivation to combine the Admitted Prior Art in view of Dunn further in view of Bliss that supports the rejection of claims 7, 21, 37, 52, 66, 82, 97, 112, 127, 141, 157, 218, 10, 24, 40, 55, 69, 85,100, 115, 130, 144, 160, 221 11, 25, 41, 56, 70, 86, 101, 116, 131, 145, 161, 222, 215, 253, 254, 257, 259, 260, 263, 265, 266, 271, 272, 275, 277, 278, 281, 283, 284, 287, 289,

290, 293, 295, 296, 299, 301, 302, 305, 307, 308, 311, 313, 314, 317, 319, 320, 323, 325, 326, 329, 331, 332, 336, 337, 338, 341, 343, 344, 347, 349, 350, 353, 355, 356 ,359 ,361, 362, 365, 367, 368, 370, 372, 374, and 376 under 35 U.S.C. §103(a). In this case, the Patent Office has made no showing of a motivation to combine based on actual, specific evidence.

With respect to the combination of Dunn and the admitted prior art, the Patent Office asserts that it "would have been obvious to one having ordinary skill in the computer art at the time Appellants made the invention to adapt the teachings of Dunn and Bliss into the prior art because Dunn enables one to improve transmission accuracy by controlling the packet format in each sessions . . . ." [*see* Final Office Action, April 20, 2005, pages 5 and 6] The Patent Office cites no evidence in support of this purported motivation. It is respectfully submitted that neither the Admitted Prior Art nor Dunn discloses or suggests that transmission accuracy can be improved by controlling the packet format in each sessions. Furthermore, the Patent Office appears to be suggesting that because Dunn "enables one to improve the transmission accuracy by controlling the packet format in each session," this is a motivation to combine the Admitted Prior Art and Dunn. This is simply not the case. The Patent Office has not suggested a motivation for combining the Admitted Prior Art, as much as the Patent Office has cited presumed benefits of the Dunn patent. The claims state that "the serial control data signal comprises during a write operation information as to a start of a sync mark and a start of write padding data, and during a read operation information that a sync mark was detected." The motivation provided by the Patent Office is just a naked assertion, completely unsupported by any actual evidence.

With respect to the combination of Bliss and the Admitted Prior Art, the Patent Office asserts that it "would have been obvious to one having ordinary skill in the computer art at the time Appellants made the invention to adapt the teachings of Dunn and Bliss into the prior art because . . . Bliss teaches one to synchronize the data stream with the sync mark." [*see* Final Office Action, April 20, 2005, pages 5 and 6] The Patent Office cites no evidence in support of this purported motivation. It is respectfully submitted that neither the Admitted Prior Art nor Bliss discloses or suggests that the data stream should be synchronized with the sync mark. Furthermore, the Patent Office appears to be suggesting that because Bliss allegedly "teaches one to synchronize the data stream with the sync mark," this is a

motivation to combine the Admitted Prior Art and Bliss. This is simply not the case. The Patent Office has not suggested a motivation for combining the Admitted Prior Art, as much as the Patent Office has cited presumed benefits of Bliss. The motivation provided by the Patent Office is just a naked assertion, completely unsupported by any actual evidence.

The simple fact is that the Patent Office has collected random pieces of prior art showing various bits and pieces of the Appellants' invention, and created motivations out of whole cloth to support combining the random pieces of prior art. This is simply impermissible. Because the Patent Office has not identified a motivation to combine which is supported by actual, specific evidence, the Patent Office has failed to establish a *prima facie* case of obviousness.

5. Since the Patent Office Has Not Provided Legally Sufficient Motivation To Combine the Admitted Prior Art with Dunn, Nor has the Patent Office Shown that the Admitted Prior Art, Dunn and Bliss Teach or Suggest all the Claim Features, the Combination of Dunn and the Admitted Prior Art Cannot Render Claims 7, 21, 37, 52, 66, 82, 97, 112, 127, 141, 157, 218 10, 24, 40, 55, 69, 85,100, 115, 130, 144, 160, 221 11, 25, 41, 56, 70, 86, 101, 116, 131, 145, 161, 222, 215, 253, 254, 257, 259, 260, 263, 265, 266, 271, 272, 275, 277, 278, 281, 283, 284, 287, 289, 290, 293, 295, 296, 299, 301, 302, 305, 307, 308, 311, 313, 314, 317, 319, 320, 323, 325, 326, 329, 331, 332, 336, 337, 338, 341, 343, 344, 347, 349, 350, 353, 355, 356 ,359 ,361, 362, 365, 367, 368, 370, 372, 374, and 376 Unpatentable Under 35 U.S.C. §103(a).

The Patent Office has failed to make any showing of a motivation based on actual, specific evidence to combine the Admitted Prior Art, Dunn, and Bliss. Furthermore, the Patent Office has failed to shown that the Admitted Prior Art, Dunn, and Bliss teaches or suggests the claim feature of a serial control data signal comprising during a write operation information as to a start of a sync mark and a start of a write padding data, and during a read operation information that a sync mark was detected. Therefore, the Patent Office has failed to make a *prima facie* case of obviousness, and it is respectfully submitted that claims 7, 21, 37, 52, 66, 82, 97, 112, 127, 141, 157, 218, 10, 24, 40, 55, 69, 85,100, 115, 130, 144, 160, 221 11, 25, 41, 56, 70, 86, 101, 116, 131, 145, 161, 222, 215, 253, 254, 257, 259, 260, 263, 265, 266, 271, 272, 275, 277, 278, 281, 283, 284, 287, 289, 290, 293, 295, 296, 299, 301,

302, 305, 307, 308, 311, 313, 314, 317, 319, 320, 323, 325, 326, 329, 331, 332, 336, 337, 338, 341, 343, 344, 347, 349, 350, 353, 355, 356 ,359 ,361, 362, 365, 367, 368, 370, 372, 374, and 376 are allowable over the Admitted Prior Art, Dunn, and Bliss. Therefore, the rejection of claims 7, 21, 37, 52, 66, 82, 97, 112, 127, 141, 157, 218, 10, 24, 40, 55, 69, 85,100, 115, 130, 144, 160, 221 11, 25, 41, 56, 70, 86, 101, 116, 131, 145, 161, 222, 215, 253, 254, 257, 259, 260, 263, 265, 266, 271, 272, 275, 277, 278, 281, 283, 284, 287, 289, 290, 293, 295, 296, 299, 301, 302, 305, 307, 308, 311, 313, 314, 317, 319, 320, 323, 325, 326, 329, 331, 332, 336, 337, 338, 341, 343, 344, 347, 349, 350, 353, 355, 356 ,359 ,361, 362, 365, 367, 368, 370, 372, 374, and 376 as allegedly being unpatentable under 35 U.S.C. §103(a) is improper and should be withdrawn.

For at least the aforementioned reasons, it is respectfully submitted that the combination of the Admitted Prior Art, Dunn, and Bliss does not render claims 7, 21, 37, 52, 66, 82, 97, 112, 127, 141, 157, 218, 10, 24, 40, 55, 69, 85,100, 115, 130, 144, 160, 221 11, 25, 41, 56, 70, 86, 101, 116, 131, 145, 161, 222, 215, 253, 254, 257, 259, 260, 263, 265, 266, 271, 272, 275, 277, 278, 281, 283, 284, 287, 289, 290, 293, 295, 296, 299, 301, 302, 305, 307, 308, 311, 313, 314, 317, 319, 320, 323, 325, 326, 329, 331, 332, 336, 337, 338, 341, 343, 344, 347, 349, 350, 353, 355, 356 ,359 ,361, 362, 365, 367, 368, 370, 372, 374, and 376 unpatentable.

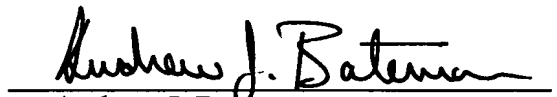
Hence, the subject matter of these claims is separately patentable for this reason.

VIII. Conclusion

For the reasons presented above, the rejections of the claims are not properly founded in the statute and should be reversed.

Respectfully submitted,

KATTEN MUCHIN ROSENMAN LLP

By: 

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APPENDIX

The Appealed Claims

1. A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that transmits a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial control data gate signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

2. A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that transmits a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

3. The latency-independent interface of claim 2, wherein the serial control data

signal comprises an amount of the data to be written during a write operation.

4. The latency-independent interface of claim 2, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

5. A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that transmits a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

6. A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that transmits a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the

data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

7. The latency-independent interface of claim 2, wherein the serial control data signal comprises:

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

8. A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that transmits a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising a ready transceiver that transmits or receives a bi-directional ready signal.

9. The latency-independent interface of claim 2, wherein the first hardware

component comprises a disk controller and the second hardware component comprises a read channel.

10. The latency-independent interface of claim 2, further comprising a sync mark transceiver that transmits or receives sync mark information.

11. The latency-independent interface of claim 10, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

12. – 14. (Canceled)

15. A latency-independent interface between first and second hardware components, comprising:

serial control transmitting means for transmitting a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

16. A latency-independent interface between first and second hardware components, comprising:

serial control transmitting means for transmitting a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

17. The latency-independent interface of claim 16, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

18. The latency-independent interface of claim 16, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

19. A latency-independent interface between first and second hardware components, comprising:

serial control transmitting means for transmitting a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

20. A latency-independent interface between first and second hardware components, comprising:

serial control transmitting means for transmitting a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

21. The latency-independent interface of claim 16, wherein the serial control data signal comprises

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

22. A latency-independent interface between first and second hardware components, comprising:

serial control transmitting means for transmitting a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising a ready transceiver means for transmitting or receiving a bi-directional ready signal.

23. The latency-independent interface of claim 16, wherein the first hardware component comprises disk controller means and the second hardware component comprises read channel means.

24. The latency-independent interface of claim 16, further comprising a sync mark transceiver means for transmitting or receiving sync mark information.

25. The latency-independent interface of claim 24, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

26. – 30. (Canceled)

31. A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

32. A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

33. The method of claim 32, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

34. The method of claim 32, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

35. The method of claim 31, A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

36. The method of claim 31, A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

37. The method of claim 32, wherein the serial control data signal comprises:

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

38. A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising the step of transmitting or receiving a bi-directional ready signal.

39. The method of claim 32, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

40. The method of claim 32, further comprising the step of transmitting or receiving sync mark information.

41. The method of claim 40, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

42. – 45. (Canceled)

46. A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that receives a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial data gate signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

47. A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that receives a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial data gate signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

48. The latency-independent interface of claim 47, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

49. The latency-independent interface of claim 47, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

50. A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that receives a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial data gate signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

51. The latency-independent interface of claim 46, A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that receives a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial data gate signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

52. The latency-independent interface of claim 47, wherein the serial control data signal comprises:

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

53. The latency-independent interface of claim 46, A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that receives a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial data gate signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising a ready transceiver that transmits or receives a bi-directional ready signal.

54. The latency-independent interface of claim 47, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

55. The latency-independent interface of claim 47, further comprising a sync mark transceiver that transmits or receives sync mark information.

56. The latency-independent interface of claim 55, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

57. – 59. (Canceled)

60. A latency-independent interface between first and second hardware components, comprising:

serial control receiving means for receiving a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the

serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

61. A latency-independent interface between first and second hardware components, comprising:

serial control receiving means for receiving a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

62. The latency-independent interface of claim 61, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

63. The latency-independent interface of claim 61, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

64. A latency-independent interface between first and second hardware

components, comprising:

serial control receiving means for receiving a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

65. A latency-independent interface between first and second hardware components, comprising:

serial control receiving means for receiving a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

66. The latency-independent interface of claim 61, wherein the serial control data signal comprises

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

67. A latency-independent interface between first and second hardware components, comprising:

serial control receiving means for receiving a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising a ready transceiver means for transmitting or receiving a bi-directional ready signal.

68. The latency-independent interface of claim 61, wherein the first hardware component comprises disk controller means and the second hardware component comprises read channel means.

69. The latency-independent interface of claim 61, further comprising a sync mark transceiver means for transmitting or receiving sync mark information.

70. The latency-independent interface of claim 69, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

71. – 75. (Canceled)

76. A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

77. A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is

one of first split, continue split and last split.

78. The method of claim 77, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

79. The method of claim 77, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

80. A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

81. A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

82. The method of claim 77, wherein the serial control data signal comprises during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

83. A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising the step of transmitting or receiving a bi-directional ready signal.

84. The method of claim 77, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

85. The method of claim 77, further comprising the step of transmitting or receiving sync mark information.

86. The method of claim 85, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

87. – 90. (Canceled)

91. A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

92. A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

93. The computer program of claim 92, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

94. The computer program of claim 92, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

95. A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

96. A computer program for transmitting and receiving signals between first and

second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

97. The computer program of claim 92, wherein the serial control data signal comprises:

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

98. A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising the step of transmitting or receiving a bi-directional ready

signal.

99. The computer program of claim 92, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

100. The computer program of claim 92, further comprising the step of transmitting or receiving sync mark information.

101. The computer program of claim 100, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

102. – 105. (Canceled)

106. A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

107. A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

108. The computer program of claim 107, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

109. The computer program of claim 107, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

110. A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

111. A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

112. The computer program of claim 107, wherein the serial control data signal comprises:

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

113. A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising the step of transmitting or receiving a bi-directional ready signal.

114. The computer program of claim 107, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

115. The computer program of claim 107, further comprising the step of transmitting or receiving sync mark information.

116. The computer program of claim 115, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

117. – 120. (Canceled)

121. A data transmission system comprising:

a first component comprising:

a serial control transmitter circuit that transmits a serial control data

signal; and

a first data transceiver circuit that transmits or receives data under the control of the serial control data signal,

a second component comprising:

a serial control receiver circuit that receives the serial control data signal; and

a second data transceiver circuit that transmits or receives the data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

122. A data transmission system, comprising:

a first component comprising:

a serial control transmitter circuit that transmits a serial control data signal; and

a first data transceiver circuit that transmits or receives data under the control of the serial control data signal; and

a second component comprising:

a serial control receiver circuit that receives the serial control data signal; and

a second data transceiver circuit that transmits or receives the data

under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

123. The latency-independent interface data transmission system of claim 122, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

124. The latency-independent interface data transmission system of claim 122, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

125. A data transmission system comprising:

a first component comprising:

a serial control transmitter circuit that transmits a serial control data signal; and

a first data transceiver circuit that transmits or receives data under the control of the serial control data signal; and

a second component comprising:

a serial control receiver circuit that receives the serial control data signal; and

a second data transceiver circuit that transmits or receives the data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

126. A data transmission system comprising:

a first component comprising:

a serial control transmitter circuit that transmits a serial control data signal; and

a first data transceiver circuit that transmits or receives data under the control of the serial control data signal; and

a second component comprising:

a serial control receiver circuit that receives the serial control data signal; and

a second data transceiver circuit that transmits or receives the data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the

data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

127. The latency-independent interface data transmission system of claim 122, wherein the serial control data signal comprises:

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

128. A data transmission system comprising:

a first component comprising:

a serial control transmitter circuit that transmits a serial control data signal; and

a first data transceiver circuit that transmits or receives data under the control of the serial control data signal; and

a second component comprising:

a serial control receiver circuit that receives the serial control data signal; and

a second data transceiver circuit that transmits or receives the data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the first component further comprises a first ready transceiver that transmits or receives a bi-directional ready signal and wherein the second component further comprising a second ready transceiver that transmits or receives the bi-directional ready signal.

129. The latency-independent interface data transmission system of claim 122, wherein said first hardware component comprises a disk controller and said second hardware component comprises a read channel.

130. The latency-independent interface data transmission system of claim 122, wherein the first component further comprises a first sync mark transceiver that transmits or receives sync mark information and wherein the second component further comprises a second sync mark transceiver that transmits or receives the sync mark information.

131. The latency-independent interface data transmission system of claim 130, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

132. – 134. (Canceled)

135. A data transmission system comprising:

first component means comprising:

serial control transmitter means for transmitting a serial control data signal; and

first data transceiver means for transmitting or receiving data under the control of the serial control data signal,

second component means comprising:

serial control receiver means for receiving the serial control data signal; and

a second data transceiver means for transmitting or receiving the data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

136. A data transmission system comprising:

first component means comprising:

serial control transmitter means for transmitting a serial control data signal; and

first data transceiver means for transmitting or receiving data under the control of the serial control data signal; and

second component means comprising:

serial control receiver means for receiving the serial control data signal; and

a second data transceiver means for transmitting or receiving the data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

137. The latency-independent interface data transmission system of claim 136, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

138. The latency-independent interface data transmission system of claim 136, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

139. A data transmission system comprising:

first component means comprising:

serial control transmitter means for transmitting a serial control data

signal; and

first data transceiver means for transmitting or receiving data under the control of the serial control data signal; and

second component means comprising:

serial control receiver means for receiving the serial control data signal; and

a second data transceiver means for transmitting or receiving the data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

140. A data transmission system comprising:

first component means comprising:

serial control transmitter means for transmitting a serial control data signal; and

first data transceiver means for transmitting or receiving data under the control of the serial control data signal,

second component means comprising:

serial control receiver means for receiving the serial control data

signal; and

a second data transceiver means for transmitting or receiving the data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

141. The latency-independent interface data transmission system of claim 136, wherein the serial control data signal comprises

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

142. A data transmission system comprising:

first component means comprising:

serial control transmitter means for transmitting a serial control data signal; and

first data transceiver means for transmitting or receiving data under the control of the serial control data signal; and

second component means comprising:

serial control receiver means for receiving the serial control data signal; and

a second data transceiver means for transmitting or receiving the data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split,

wherein said first component means further comprises first ready transceiver means for transmitting or receiving a bi-directional ready signal, and

wherein said second component means further comprises second ready transceiver means for transmitting or receiving the bi-directional ready signal.

143. The latency-independent interface data transmission system of claim 136, wherein said first hardware component comprises disk controller means and said second hardware component comprises read channel means.

144. The latency-independent interface data transmission system of claim 136, wherein said first component means further comprises first sync mark transceiver means for transmitting or receiving sync mark information, and wherein said second component means further comprises second sync mark transceiver means for transmitting or receiving the sync mark information.

145. The latency-independent interface data transmission system of claim 144,

wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

146. – 150. (Canceled)

151. A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

152. A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

153. The method of claim 152, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

154. The method of claim 152, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

155. A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

156. A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

157. The method of claim 152, wherein the serial control data signal comprises

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

158. A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising the step of transmitting or receiving a bi-directional ready signal by the first component and transmitting or receiving the bi-directional ready signal by the second component.

159. The method of claim 152, wherein said first hardware component comprises a disk controller and said second hardware component comprises a read channel.

160. The method of claim 152, further comprising the step of transmitting or receiving sync mark information by the first component, and transmitting or receiving the sync mark information by the second component.

161. The method of claim 160, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

162. – 211. (Canceled)

212. A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

213. A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

214. The computer program of claim 213, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

215. The computer program of claim 213, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

216. A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

217. A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding

serial control data is a continuation of a current serial control data.

218. The computer program of claim 213, wherein the serial control data signal comprises

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

219. A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising the step of transmitting or receiving a bi-directional ready signal by the first component and transmitting or receiving the bi-directional ready signal by the second component.

220. The computer program of claim 213, wherein said first hardware component comprises a disk controller and said second hardware component comprises a read channel.

221. The computer program of claim 213, further comprising the step of transmitting or receiving sync mark information by the first component, and transmitting or receiving the sync mark information by the second component.

222. The computer program of claim 221, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

223. – 248. (Canceled)

249. The latency-independent interface of claim 5, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

250. The latency-independent interface of claim 5, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

251. The latency-independent interface of claim 5, wherein the serial control data

signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

252. The latency-independent interface of claim 5, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

253. The latency-independent interface of claim 5, further comprising:

a sync mark transceiver that transmits or receives sync mark information.

254. The latency-independent interface of claim 253, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

255. The latency-independent interface of claim 6, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

256. The latency-independent interface of claim 6, wherein the serial control data

signal comprises an amount of the data to be read during a read operation.

257. The latency-independent interface of claim 6, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

258. The latency-independent interface of claim 6, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

259. The latency-independent interface of claim 6, further comprising:

a sync mark transceiver that transmits or receives sync mark information.

260. The latency-independent interface of claim 259, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

261. The latency-independent interface of claim 8, wherein the serial control data

signal comprises an amount of the data to be written during a write operation.

262. The latency-independent interface of claim 8, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

263. The latency-independent interface of claim 8, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

264. The latency-independent interface of claim 8, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

265. The latency-independent interface of claim 8, further comprising:

a sync mark transceiver that transmits or receives sync mark information.

266. The latency-independent interface of claim 265, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of

padding data.

267. The method of claim 35, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

268. The method of claim 35, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

269. The method of claim 35, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

270. The method of claim 35, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

271. The method of claim 35, further comprising the step of:

transmitting or receiving sync mark information.

272. The method of claim 271, wherein during a write operation a first assertion of

the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

273. The method of claim 36, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

274. The method of claim 36, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

275. The method of claim 36, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

276. The method of claim 36, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

277. The method of claim 36, further comprising the step of:

transmitting or receiving sync mark information.

278. The method of claim 277, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

279. The method of claim 38, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

280. The method of claim 38, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

281. The method of claim 38, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

282. The method of claim 38, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

283. The method of claim 38, further comprising the step of:

transmitting or receiving sync mark information.

284. The method of claim 283, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

285. The latency-independent interface of claim 50, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

286. The latency-independent interface of claim 50, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

287. The latency-independent interface of claim 50, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

288. The latency-independent interface of claim 50, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

289. The latency-independent interface of claim 50, further comprising:

a sync mark transceiver that transmits or receives sync mark information.

290. The latency-independent interface of claim 289, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

291. The latency-independent interface of claim 51, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

292. The latency-independent interface of claim 51, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

293. The latency-independent interface of claim 51, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

294. The latency-independent interface of claim 51, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read

channel.

295. The latency-independent interface of claim 51, further comprising:

a sync mark transceiver that transmits or receives sync mark information.

296. The latency-independent interface of claim 295, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

297. The latency-independent interface of claim 53, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

298. The latency-independent interface of claim 53, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

299. The latency-independent interface of claim 53, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

300. The latency-independent interface of claim 53, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

301. The latency-independent interface of claim 53, further comprising:

a sync mark transceiver that transmits or receives sync mark information.

302. The latency-independent interface of claim 301, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

303. The method of claim 80, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

304. The method of claim 80, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

305. The method of claim 80, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write

padding data; and

during a read operation, information that a sync mark was detected.

306. The method of claim 80, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

307. The method of claim 80, further comprising the step of:

transmitting or receiving sync mark information.

308. The method of claim 307, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

309. The method of claim 81, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

310. The method of claim 81, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

311. The method of claim 81, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

312. The method of claim 81, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

313. The method of claim 81, further comprising the step of:

transmitting or receiving sync mark information.

314. The method of claim 313, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

315. The method of claim 83, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

316. The method of claim 83, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

317. The method of claim 83, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

318. The method of claim 83, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

319. The method of claim 83, further comprising the step of:

transmitting or receiving sync mark information.

320. The method of claim 319, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

321. The data transmission system of claim 125, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

322. The data transmission system of claim 125, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

323. The data transmission system of claim 125, wherein the serial control data

signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

324. The data transmission system of claim 125, wherein said first hardware component comprises a disk controller and said second hardware component comprises a read channel.

325. The data transmission system of claim 125, wherein the first component further comprises a first sync mark transceiver that transmits or receives sync mark information, and

wherein the second component further comprises a second sync mark transceiver that transmits or receives the sync mark information.

326. The data transmission system of claim 325, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

327. The data transmission system of claim 126, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

328. The data transmission system of claim 126, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

329. The data transmission system of claim 126, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

330. The data transmission system of claim 126, wherein said first hardware component comprises a disk controller and said second hardware component comprises a read channel.

331. The data transmission system of claim 126, wherein the first component further comprises a first sync mark transceiver that transmits or receives sync mark information, and

wherein the second component further comprises a second sync mark transceiver that transmits or receives the sync mark information.

332. The data transmission system of claim 331, wherein during a write operation a

first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

333. The data transmission system of claim 128, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

334. The data transmission system of claim 128, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

335. The data transmission system of claim 128, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

336. The data transmission system of claim 128, wherein said first hardware component comprises a disk controller and said second hardware component comprises a read channel.

337. The data transmission system of claim 128, wherein the first component further comprises a first sync mark transceiver that transmits or receives sync mark

information, and

wherein the second component further comprises a second sync mark transceiver that transmits or receives the sync mark information.

338. The data transmission system of claim 331, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

339. The method of claim 155, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

340. The method of claim 155, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

341. The method of claim 155, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

342. The method of claim 155, wherein said first hardware component comprises a disk controller and said second hardware component comprises a read channel.

343. The method of claim 155, further comprising the steps of:

transmitting or receiving sync mark information by the first component; and

transmitting or receiving the sync mark information by the second component.

344. The method of claim 343, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

345. The method of claim 156, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

346. The method of claim 156, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

347. The method of claim 156, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

348. The method of claim 156, wherein said first hardware component comprises a

disk controller and said second hardware component comprises a read channel.

349. The method of claim 156, further comprising the steps of:

transmitting or receiving sync mark information by the first component; and

transmitting or receiving the sync mark information by the second component.

350. The method of claim 349, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

351. The method of claim 158, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

352. The method of claim 158, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

353. The method of claim 158, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

354. The method of claim 158, wherein said first hardware component comprises a disk controller and said second hardware component comprises a read channel.

355. The method of claim 158, further comprising the steps of:

transmitting or receiving sync mark information by the first component; and

transmitting or receiving the sync mark information by the second component.

356. The method of claim 355, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

357. The latency-independent interface of claim 1, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

358. The latency-independent interface of claim 1, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

359. The latency-independent interface of claim 1, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

360. The latency-independent interface of claim 1, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

361. The latency-independent interface of claim 1, further comprising:

a sync mark transceiver that transmits or receives sync mark information.

362. The latency-independent interface of claim 361, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

363. The method of claim 31, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

364. The method of claim 31, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

365. The method of claim 31, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

366. The method of claim 31, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

367. The method of claim 31, further comprising the step of:

transmitting or receiving sync mark information.

368. The method of claim 367, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

369. The latency-independent interface of claim 46, wherein the serial control data signal comprises one of an amount of the data to be written during a write operation and an amount of the data to be read during a read operation.

370. The latency-independent interface of claim 46, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write

padding data; and

during a read operation, information that a sync mark was detected.

371. The method of claim 76, wherein the serial control data signal comprises one of an amount of the data to be written during a write operation and an amount of the data to be read during a read operation.

372. The method of claim 76, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

373. The data transmission system of claim 121, wherein the serial control data signal comprises one of an amount of the data to be written during a write operation and an amount of the data to be read during a read operation.

374. The data transmission system of claim 121, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

375. The method of claim 151, wherein the serial control data signal comprises one of an amount of the data to be written during a write operation and an amount of the data to be read during a read operation.

376. The method of claim 151, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.